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A Thesis

*Submitted in partial fulfillment of the requirements
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BY

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(ROLL NO.)



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA-835215, RANCHI**

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ABSTRACT

The major design metric for designing a basic SRAM cell include high value of RSNM, low power consumption and higher reliability. Whereas a radiation tolerant SRAM cell includes the design metric of soft error robustness. In this paper, we have proposed a Quad-node 10 transistor (10T) SRAM cell which has more soft error robustness than the Quatro 10T cell. The NMOS access transistors of the Quatro 10T cell are replaced by the PMOS access transistors in the proposed 10T cell. The benefit of using PMOS access transistors is due to its high radiation tolerance. The leakage currents in PMOS access transistors are not affected by the radiation bombardment. Whereas they increase rapidly in NMOS transistors. In hold operation, both the cells consume same amount of power as the access transistors are cutoff. We also have smaller gate leakages in the case of PMOS access transistors than NMOS access transistors. In the case of hold operation, both the Quatro and proposed cells are able to recover 1→0 single event transients (SET). For 0→1 single event transients (SET) in hold operation, proposed cell shows an increment of 3 μ A in current margin. This improves the hold failure probability of the proposed cell. The increment in current margin is obtained by compromising the increment in the value of read access time by 2.04%. Rest of the design matrices such as Read Static Noise Margin (RSNM), Hold power, Write Static Noise Margin (WSNM) and Cell Area remains same.

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Thank you.

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CHAPTER 1

RADIATION HARDENED CELL

1.1 INTRODUCTION

Excessive demand of Electronic gadgets has led to a new revolution in the field of VLSI technology. These devices are replacing the basic amenities of human life and therefore need to be upgraded for various improvements with the passage of time. Application of VLSI technology is widely spread to various electronic devices from a simple mobile to smart phones, GPS positioning systems, defense and military operations, global communication systems, radars, satellites, medical services and is still not limited. Most of the applications in VLSI possess memories as their integral part to perform various functions and to store the data wherever it is required. Memories play a vital role in making the system intelligent. There are numerous categories of memory to be used in various operations and may possess permanent storage or temporary storage with static or dynamic operations.

Static Random Access Memory (SRAM) is a type of volatile memory, which means it can only store data when its power supply is turned on. When the power is turned off, the data will be lost. The users can read any data given the address of the data, or the users can write data to a specific address. It is an important component of integrated circuits and Systems on Chip (SoC). It occupies a large portion of the total-die area and it is also predicted that nearly 94% of the total die area would be occupied by onchip cache memory in near future nano-scale technologies. It's faster read and write speed compared to other type of memories makes it desirable in many speed contingent applications. They are widely used for register files and memory caches. They are composed of a memory bitcell array, address decoders (column and row decoders), multiplexers, sense amplifiers, write drivers and pre-charged circuits. However, there are drawbacks of SRAM, with one being the large area penalty and another being the susceptibility to radiation damage.

Almost forty years ago, the effects of radiation on semiconductor devices were observed when the first satellite experienced serious problems caused by the high energy particles. Before the 1970's, the effects of radiation events on ICs were considered only in mission critical applications for space and military projects, where the reliability of the system was more important than area minimization and speed requirements, that are demanded by commercial applications. During the 1980's, several reports were published showing evidence of radiation strike effects on commercial VLSI circuits in terrestrial environment.

Electronic systems operating in radiation environment are increasingly vulnerable to radiation effects, due to fabrication process scaling, decreasing feature sizes, supply voltages and lower noise margins. Single event effects (SEEs) are caused when radiation particles such as protons, neutrons, alpha particles, or heavy ions strike sensitive diffusion regions of transistors in circuits. Studies have shown that SEEs are troublesome for military and space applications and radiation-induced single-event transients (SET) were the primary failure mechanism behind several spacecraft malfunctions in recent years [1-4]. There are also critical applications like biomedical, industrial and banking systems that also demand highly reliable systems [5].

1.2. MECHANISM OF RADIATION HARDENED CELL

SRAMs (Static Random Access Memories) have lower supply voltage and smaller node capacitance, which makes it more susceptible to radiation particles, such as alpha particles, heavy ion and cosmic rays. Due to low signal charge and reduced noise margin, nanoscale integrated circuits are extremely susceptible to particle-induced single event transients (SETs). Primarily, SETs are caused by alpha particles and cosmic neutrons, which originate from packaging materials and intergalactic rays, respectively. Through direct or indirect ionization in silicon, these particles generate extra charge, which gets collected by sensitive nodes and creates voltage transients at those nodes. A latch consists of a cross-coupled inverter pair. When the amplitude and duration of the transient is large, it alters the stored value in the latch, causing a single event upset (SEU). A SEU is also referred to as a 'soft error' as it does not permanently damage the device. However, soft error can lead to system malfunctions and can disturb the state of

SRAMs. When radiation particles pass through the sensitive node of SRAMs, it will release electron-hole pairs along its path. Under the action of electric field, the holes move toward the source region of the transistor, while the electrons move toward the drain region end of the transistor. When these electrons are accumulated to a certain extent, the stored state in this sensitive node will be changed. In order to limit the SRAM SER, error correction codes (ECC) or soft error hardened memory cells are used.

1.3. FUNDAMENTALS OF SOFT ERRORS

The prediction and study of soft errors in electronics can be dated back to the 60s. In 1961, J. T. Wallmark first raised the issue of soft errors in [2]. In 1975, four “anomalies” were found in satellites and reported in [3]. In 1979, Intel Corp. found soft errors in Dynamic Random Access Memory (DRAM). As the microelectronic circuits continue to shrink in size, soft errors have become an increasingly important issue. In the past decade, many telecommunication companies have suffered from soft errors and have dedicated significant customer services to this. For instance, the high end server crash from Sun Microsystems is reported in [4]; Cisco’s network glitch in 2005 had significant financial consequences [5]. The Semiconductor Industry Association (SIA) roadmap has identified soft errors as the major threat to reliable operation of electronic systems in the future [6]. Therefore, much research has been conducted to study the soft errors mechanism in analog and digital circuits.

1.4 MECHANISM OF SOFT ERRORS

Both “single event transient” (SET) and “single event upset” (SEU) can be categorized as soft errors. SET is an undesirable transient pulse usually generated in combinational logic circuits under radiation strike and propagates through the logic chain, in which the output is based on a logical relation to the inputs with no capability of retention. If a SET propagates to the input of a latch or a flip-flop during a latching clock signal, the erroneous input will be latched and stored and this causes a SEU. In older technologies, a SET is hard to propagate because it usually does not produce a full output swing or is quickly attenuated because of large load capacitances and large propagation delays. In advanced

technologies, where the propagation delay is reduced and the clock frequency is high, SET can traverse many logic gates easily, and the probability that a SET is locked in a latch and causes SEU increases. It should be noted that there is another similar effect that is caused by radiation in electronics called Single Event Latch-up (SEL). The mechanism of SEL is the same as a classical electrical latch-up. A SEL can result in a high operating current, and it must be cleared by resetting the power. SELs can also cause permanent damage to the device if the latch-up current is very high. Figure 1.1 (a) shows a scenario when a ray of radiation strikes the drain area of an N-type Metal Oxide Semiconductor (NMOS) transistor [7]. As can be seen in Figure 1.1 (a), the radiation brings in different charge (positive and negative). If the radiation particle is a proton or a neutron, it can react with the silicon nuclei and create secondary charge. The nature of the built-in electric field in the PN junction between the drain area and the substrate of the NMOS transistor leads to the negative charge being collected in the N+ diffusion area and the positive charge being deposited at the substrate, as shown in Figure 1.1 (b). Therefore, a transient current spike can be observed at the drain node, as shown in Figure 1.1 (d). The current spike can consequently induce a voltage spike. The voltage spike is undesirable and can be locked by any memory or latch unit. Eventually the charge collected at the drain and the substrate will diffuse and get neutralized over time as can be seen in Figure 1.1 (c).

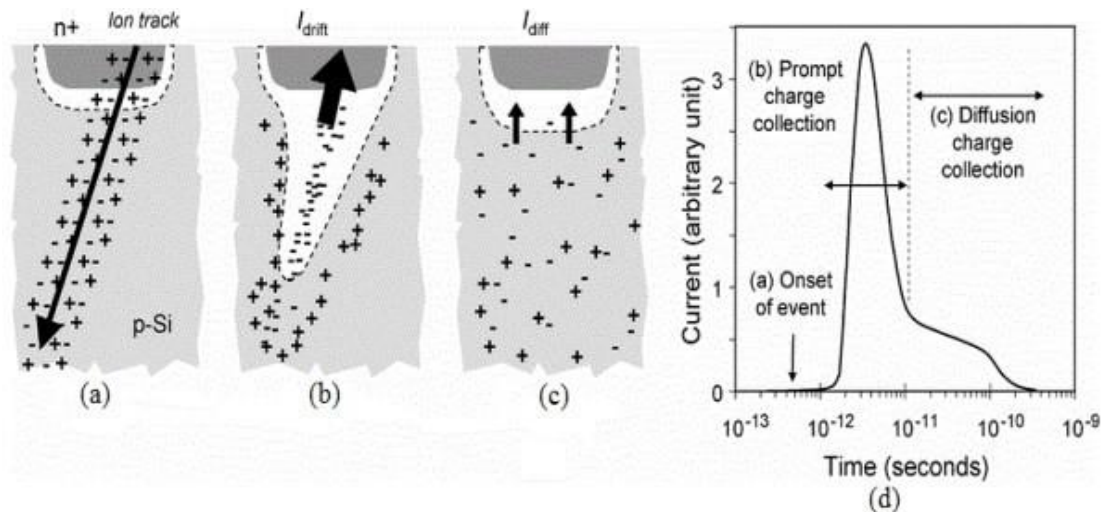


Figure 1.1 Charge generation and collection in a PN junction

1.5. SOURCES OF SOFT ERRORS

Sources of soft errors can come from the packaging material of the chip, terrestrial environment and space environment. In different environments, different radiation sources cause the soft errors. The most common sources of the soft errors are “alpha particle”, “proton”, “neutron” and “heavy ions”. The following is an introduction of these sources of soft errors and how they cause “upsets” in integrated circuits.

1.5.1. ALPHA PARTICLE

An alpha particle is composed of two protons and two neutrons, and it can be emitted from unstable radioactive isotopes. The most common radioactive isotopes are Uranium-235, Uranium-238, and Thorium-232. They can be found in commonly used packaging materials of integrated circuit chips. These radioactive isotopes can release energies within the range from 4 MeV to 9 MeV. The soft errors in DRAM found by Intel in the late 1970s were caused by traces of Uranium and Thorium in the packaging materials. Since the alpha particle carries a positive charge, it can create an ionized path as it travels through the silicon until it loses all of its energy. The higher the energy, the further it travels. The usual travel length of an alpha particle with less than 10 MeV energy is < 100 μm . Therefore, the alpha particle outside of the package material is not a concern for soft errors. Currently, many foundries have reduced or eliminated the radioactive isotopes in the packaging material, and soft errors caused by alpha particles are subsequently reduced.

1.5.2. NEUTRON

Neutrons are one of the major sources of soft errors in a terrestrial environment. They originate from the near-earth space environment. In the near-earth space environment, neutrons usually have very high energy, and they can react with the upper atmosphere of the earth. The reacting collisions, modulated by the earth’s magnetic field, can generate high-energetic recoil particles, such as high energy neutrons, muons and pions. Out of these particles, only the charge-less high energy neutrons have the potential to reach the earth’s surface to interact with semiconductor devices. The remaining energy is about 1- 500 MeV when they

reach the earth's surface. The terrestrial radiation environment consists of about 92 % neutrons, 4 % pions and 2 % protons [8]. For a high-energy neutron to cause a soft error, it must produce ionized particles by colliding with the silicon nucleus and undergo impact ionization with the silicon nuclei. This kind of collision generates alpha particles and other heavier ions, producing electron-hole pairs, but with higher energies than a typical alpha particle from packaging impurities. In 1993, the neutron-induced soft errors were found in a computer onboard a commercial aircraft [10].

1.5.3. PROTON

High energy protons are the biggest concern for soft errors in the near-earth space environment. Protons have the same indirect ionization mechanism as neutrons. The details of proton-induced soft errors are investigated in [11]-[17]. A proton carries a positive charge, but the indirect ionization between the proton and silicon nuclei can actually generate a lot more charge than that from a proton itself. High energy protons can also be generated by a reaction between heavy ions and silicon dopants. Elastic scattering and spallation reactions between Si (p, p) Si²⁸, Si (p, He⁴) Mg²⁵, and Si²⁸ (p, p He⁴) Na²⁴ can transfer a large fraction of proton energy to the recoils and fragments [18]. In the terrestrial environment, low energy protons are usually absorbed in the atmosphere or shielded by the package of the circuit chip, and therefore do not pose soft error threats.

1.5.4. HEAVY IONS

A heavy ion by definition is any ion that has more than two atoms. It is a major source of the soft errors in the space environment, and it has very high Linear Energy Transfer (LET) level. LET is used to measure the energy of a radiation strike and it is measured in terms of energy lost per unit length. A heavy ion can cause the soft errors via direct ionization. Heavy ions are abundant in cosmic rays in the space environment. The effects heavy ions have on integrated circuits have been observed in space and aircraft electronics. Some heavy ions can also react with silicon dopants (especially Borons) to generate neutrons and protons.

1.6. LITERATURE REVIEW

Under radiation environment, conventional SRAMs suffer from high soft-error rate. To address this challenge, several radiation-hardened static-random accessmemory (SRAM) cells such as twelve-transistor (12T) Dice and ten-transistor (10T) Quatro have been developed. Quatro is more promising since this cell delivers robust operation while incurring moderate area overhead. However, our study shows that Quatro experiences large number of write failures under parametric variations of scaled technologies, impeding the application of this SRAM cell. Continuous transistor scaling, coupled with the growing demand for low-voltage, low-power applications, increases the susceptibility of VLSI circuits to soft-errors, especially when exposed to extreme environmental conditions, such as those encountered by space applications. The most vulnerable of these circuits are memory arrays that cover large areas of the silicon die and often store critical data. Radiation hardening of embedded memory blocks is commonly achieved by implementing extremely large bitcells or redundant arrays and maintaining a relatively high operating voltage; however, in addition to the resulting area overhead, this often limits the minimum operating voltage of the entire system leading to significant power consumption.

Paper1- A Soft Error Tolerant 10T SRAM Bit-Cell with Differential Read Capability- by Shah M. Jahinuzzaman, David J. Rennie and Manoj Sachdev, - A 10T SRAM cell is proposed that reduces soft errors by 98% and facilitates a differential read access. Differential read is critical for easier design of the sense amplifier and for reliable sense operation under the worst case conditions. The high SNM of the proposed cell enables operating in sub-0.4 V regime to save leakage power while offering better data stability compared to the 6T cell as well as the DICE cell. In addition, the cell can be used as a latch to design soft error robust register files and flip-flops. A quad-node ten transistor (10T) soft error robust SRAM cell offers differential read operation for robust sensing. The cell exhibits larger noise margin in sub-0.45 V regime and 26% less leakage current than the traditional soft error tolerant 12T DICE SRAM cell. When compared to a conventional 6T SRAM cell, the proposed cell offers similar noise margin as the 6T cell at half the supply voltage, thus significantly saving the leakage power.

Paper 2- Process Variation and Radiation-Immune Single Ended 6T SRAM Cell- by A. Islam and M. Hasan- This paper presents a PFET-based single ended 6T SRAM cell which is radiation hardened and capable of saving write dynamic power. It has successfully demonstrated that the proposed design is robust against the impact of process, voltage and temperature variations in terms of tighter spread in write EDP. The simulation measurement results confirm the successful functionality and read/write stability of the proposed design. The benefits of read and write power reduction make it an attractive choice for applications where static noise is negligible. The leakage power can dominate the system power dissipation and determine the battery life in battery-operated applications with low duty cycles, such as the wireless sensors, cellular phones, PDAs or pacemakers. Driven by the need of ultra-low power applications, this paper presents single ended 6T SRAM (static random access memory) cell which is also radiation hardened due to maximum use of PMOS transistors. Due to process imperfection, starting from the 65 nm technology node, device scaling no longer delivers the power gains. Since then the supply voltage has remained almost constant and improvement in dynamic power has stagnated, while the leakage currents have continued to increase. Therefore, power reduction is the major area of concern in today's circuit with minimum geometry devices such as nanoscale memories. The proposed design in this paper saves dynamic write power more than 50%. It also offers 29.7% improvement in TWA (write access time), 38.5% improvement in WPWR (write power), 69.6% improvement in WEDP (write energy delay product), 26.3% improvement in WEDP variability, 5.6% improvement in RPWR (read power) at the cost of 22.5% penalty in SNM (static noise margin) at nominal voltage of $V_{DD} = 1$ V. The tighter spread in write EDP implies its robustness against process and temperature variations. Monte Carlo simulation measurements validate the design at 32 nm technology node.

Paper 3- Leakage Characterization of 10T SRAM Cell- by A. Islam and M. Hasan- —This paper presents a technique for designing a low-power and variability-aware SRAM cell. The cell achieves low power dissipation due to its series-connected tail transistor and read buffers, which offer a stacking effect. This paper studies the impact of process, voltage, and temperature (PVT) variations on most of the design metrics of the SRAM cell and compares the

results with standard 6T, 9T, and ST10T (Schmitt trigger based) SRAM cells. It proposes a low-power variability-aware 10T SRAM cell. It analyzes the impact of PVT variations on read/write delay and standby power. The results show significant improvement in most of the design metrics over standard 6T, 9T, and ST10T SRAM cells, demonstrating its robustness and low-power operability. The proposed design is, therefore, an attractive choice for low-power applications in scaled technology in the presence of PVT variations.

Paper 4- Radiation Hardened Area-Efficient 10T SRAM Cell for Space Applications- by Sayeed Ahmad, Naushad Alam and Mohd Hasan- Under the influence of continuous CMOS scaling, SRAMs are facing severe reliability challenges due to high energy particle's strike in radiation environment. This brief presents a novel radiation-hardened 10T SRAM cell with very low area overhead. The HSPICE simulation results carried out using double exponential current source model demonstrate that proposed cell not only fully recovers single-event upsets (SEUs) at any of its sensitive node but also tolerates singleevent multi-node upsets (SEMNU) on two fixed nodes independent of the stored value. The simulation results also confirm that the proposed cell shows improved hold/read static noise margin, smaller write delay, consumes low leakage power at the cost of low write margin compared with most of the other radiation hardened cells. At the same time, it shows only 66% area overhead compared with 6T cell, whereas most of the other radiation hardened cells show more than 95% area overhead. Therefore the proposed cell could be a good choice for aerospace applications that demand high read stability, low leakage and stringent area requirement. This work proposed a novel radiation-hardened 10T SRAM cell with very low area overhead. The HSPICE simulation carried out using double exponential current source model demonstrated the capability of proposed cell for fully tolerating SEU at any of its sensitive node and also tolerating SEMNU on two fixed nodes independent of the stored value. The simulation results presented that the proposed cell introduced penalty of

degraded write-margin. However its other attractive features such as fully SEU tolerance, low leakage, low area and high HSNM/RSNM, make it a possible choice for aerospace applications that demand high read stability, low leakage and stringent area requirement.

Paper 5- Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application- by Chunyu Peng, Jiati Huang, Changyong Liu, Qiang Zhao, Songsong Xiao, Xiulong Wu, Zhiting Lin, Junning Chen, and Xuan Zeng- In this paper, a novel radiation-hardened 14-transistor SRAM bitcell with speed and power optimized [radiation-hardened with speed and power optimized (RSP)-14T] for space application is proposed. By circuit- and layout-level optimization design in a 65-nm CMOS technology, the 3-D TCAD mixed-mode simulation results show that the novel structure is provided with increased resilience to single-event upset as well as single-event-multiple-node upsets due to the charge sharing among OFF-transistors. Moreover, the HSPICE simulation results show that the write speed and power consumption of the proposed RSP-14T are improved by $\sim 65\%$ and $\sim 50\%$, respectively, compared with those of the radiation hardened design (RHD)-12T memory cell. In this paper, the radiation-hardened 14T SRAM bitcell with speed and power optimized (RSP-14T) based on the source isolation technique is presented. Through the circuit- and layout-level optimization, the mixed-mode simulation results show that it can not only tolerate an SEU on any of its inner single node, but also have partial SEMNUs immune even at the LET value equal to $60 \text{ MeVcm}^2/\text{mg}$, which is larger than that reported for RHD-12T. Meanwhile, compared with RHD12T, its write speed and power consumption are significantly improved. Thus, the excepting area increased slightly, and the proposed RSP14T cell is more suitable for the space application.

1.7. MOTIVATION

With CMOS technologies scaling down, $0.18 \mu\text{m}$ and $0.13 \mu\text{m}$ CMOS processes have become the main-stream technologies used in commercial products. The radiation hardness perspectives for design of analog detector readout circuits in the $0.18 \mu\text{m}$ CMOS technology have been investigated by some researchers. It shows that the increase of the leakage component in the NMOS drain-source current may affect the behavior of devices used for logic or switching functions

in radiation environments. SRAMs are often the most sensitive blocks to radiation strikes, where the ions can easily deposit charge on the storage node of these memory cells, corrupting the data stored in them. The errors then will be stored in the memory, unless they are identified and rewritten with the correct data. Hence upsets in memories are considered more critical than the ephemeral single event transients occurring in combinational circuits.

1.8. OBJECTIVE

The objective of this thesis is to design a radiation hardened and soft error tolerant SRAM bitcell structures that has less leakage current. Both schematic and layout approach are used in designing bitcells. Since SRAMs are widely used in memory caches, register files and SoCs, the data in the SRAMs can be severely corrupted under radiation strikes; therefore, it is important to design a SRAM that is robust in a radiation environment. In this thesis, a soft error robust SRAM bitcell design is proposed and a RHBD approach is adopted to further improve the soft errors tolerance. To evaluate the proposed SRAM bitcell design, a test chip is fabricated using 22 nm CMOS technology in Hspice. Different experiments (Read Access Time, Hold Power, Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM) and Soft Error Robustness) have been carried out for evaluations, and comparison between simulation and experiments are presented in this thesis.

1.9. THESIS ORGANIZATION

This thesis is organized as follows:

CHAPTER 1: This chapter gives an overview of radiation hardened cell, Literature Review, Motivation and Objective of the thesis.

CHAPTER 2: This chapter includes radiation environment

CHAPTER 3: This chapter discusses Radiation Hardened By Design (RHBD)

CHAPTER 4: This chapter discusses existing SRAM bitcell designs

CHAPTER 5: This chapter discusses proposed cell, operations and result

CHAPTER 6: This chapter summarizes and suggests future scope to improve this research work.

CHAPTER 2

RADIATION ENVIRONMENTS

2.1 INTRODUCTION

In this section, a brief overview of the various environments likely to have a degrading effect on electronic devices and systems is presented. It includes space, ground level, nuclear reactors, radiation processing, weapons and highenergy physics experiments.

2.1.1 THE SPACE ENVIRONMENT

The space radiation environment is composed of a variety of energetic particles with energies ranging from keV to GeV and beyond. These particles are either trapped by the Earth's magnetic field or are passing through the solar system. The main elements of the radiation environment are: the radiation belts, cosmic rays, and solar flares.

- The radiation belts. This consists of many different types of energetic charged particles trapped in the Earth's magnetic field, forming the radiation belts. It consists mainly of electrons of energy up to a few MeV and protons up to several hundred MeV.
- Cosmic rays. These are low fluxes of energetic heavy ions extending to energies beyond TeV and including all ions in the periodic table. There are three sources of cosmic rays: galactic, solar and terrestrial. Galactic cosmic rays are 'primary' cosmic rays which originate outside the solar system but are associated with the galaxy and provide a continuous low-flux component of the radiation environment. They are comprised of about 85 per cent protons, 14 per cent alpha particles and 1 per cent heavier nuclei with energies extending to 1 GeV. Solar cosmic rays not only produce an intensive burst of both UV and X-rays, but also accelerate solar material to high velocities. These solar particles are similar to galactic cosmic rays but, due to their different origin, are not identical in composition. The primary cosmic radiation which penetrates the Earth's atmosphere is rapidly transformed by interactions which

produce a cascade of secondary radiation. These cascades take place in the main body.

- Solar flares. Protons from solar flare, together with electrons and alpha particles in smaller quantities, are emitted by the sun in bursts during solar storms. Their fluxes, besides being intermittent, vary overall with the solar cycle.

In addition, space is pervaded by plasma of electrons and protons with energies up to about 100 keV. Within the trapped radiation belts, these particles merely represent the low-energy extremes of the trapped electron and proton populations. In the outer zones of the magnetosphere and in interplanetary space, these particles are associated with the solar wind, and considerable fluxes will be encountered at very high altitudes. The low energy particles are easily stopped by very thin layers of material and hence only the outer-most surfaces such as thermal control material and solar cell cover slips are affected. The low-energy plasma can cause spacecraft charging and the internal electronics may be affected by this charging and subsequent discharging.

The electronics in space experiences two types of radiation effects: one is caused by the accumulation of ionization over a period of time, which eventually leads to performance degradation and/or functional failure. The other one is due to a single high-energy particle as it strikes the sensitive nodes (or sensitive volumes) within the electronic device. It is primarily the results of currents generated as an energetic particle passes through circuit elements (the radiation effects on electronics are fully explained in next chapter). This type of effect is the main problem that needs to be addressed by the space community. There are two approaches for choosing the electronics in radiation environments: the first one uses qualified radiation-hard electronics; the second one uses commercial electronics, the so-called radiation tolerant electronics, which has to be evaluated by the customer.

In conclusion, the space environment has a very wide range of radiation levels depending on the type of space missions. The electronics in each mission will endure different doses of radiation introduced by various fluxes of particles.

2.2.2. THE GROUND LEVEL

The radiation effects on VLSI at ground level were first reported by T. May and M. Woods, in discovering errors in RAM chips due to upsets caused by the alpha particles released by the contaminants within the chip packaging material. Chip vendors managed to find some specific solutions to reduce them to tolerable levels, mainly by reducing the alpha particle flux emitted by packaging and processing materials. On the other hand, cosmic rays also exist on the ground, even if their intensity and energy are reduced compared to those of in the space. The secondary particles produced by cosmic rays are primarily neutrons. The others include protons and p-ions. The atmospheric neutrons are believed to be the major cause of the upsets occurring in VLSI. The neutron environment at ground level can be defined in terms of the models for the atmospheric neutron flux at higher altitudes which are mainly based on neutrons in the energy range of greater than 1 MeV and less than 10 MeV. It is shown by a number of studies that the shape of the energy spectrum of the atmospheric neutron flux does not change with altitude or latitude, even though its absolute magnitude does vary with location and altitude around the Earth. Some data shows that 10-100 MeV flux of neutrons falls off approximately linearly with altitude. Very few measurements of the neutron spectrum at ground level have been made. However, one set of most recent terrestrial spectral measurements shows that the ground spectrum is roughly 1/300 of that at 40,000 ft. An upset rate in the range of $1-2 \times 10^{-12}$ upset/bithour was shown to be representative of the rate that most SRAMs and DRAMs in actual field applications are experiencing. The impact due to the upsets caused by the neutrons, include: improving the reliability of large computer system; applying error mitigation techniques to RAMs used in biomedical, commercial, and industrial products, etc.

2.2.3. THE NUCLEAR REACTOR ENVIRONMENT

Three levels of radiation severity need to be considered for nuclear fission power plants: within the reactor core and cavity, in the containment, in the containment under accident conditions.

The major radiation sources in the reactor environment are neutrons and gamma rays (Kak86). The most important environment for equipment and components is

‘in containment’ and, while the gamma dose rate and neutron flux are moderate, the requirement for 40 years operating life results in significant accumulated levels. Safety equipment is required to operate at the end of a specified lifetime. Such equipment must also operate during and after a radioactive accident. Other stress factors must be taken into account in conjunction with radiation effects in order to arrive at a true estimate of the life expectancy and to define adequate qualification tests.

2.2.4. THE RADIATION PROCESSING ENVIRONMENT

Radiation processing is a branch of radiation technology, which involves the deliberate introduction of radiation damage into materials for beneficial purposes. The aspect of radiation processing which has caught the attention of the public in recent years concerns the irradiation of food products in order to eradicate harmful organisms and extend shelftime. This is a small part of what is now becoming a major application in industry. Examples include the following:

- Modern consumer-oriented society generates a large amount of waste, and radiation processing is a potential solution for many of the problems involved in waste treatment and the cleansing of water supplies.
- Radiation processing is used in the medical field for the sterilization of a number of products such as dressings, hypodermic needles, and catheters.
- Industrial applications are increasing, particularly in the field of materials modification. The polymer industry uses radiation for the cross-linking of polymers to produce durable insulation for wires and cables particularly for submarine use. Current investigations center around polymer grafting, with reference to the controlled delivery of drugs.
- The semiconductor industry is beginning to use radiation processing for the modification of starting materials, particularly silicon.
- Many developing nations benefit from radiation processing. The economy of such nations frequently depends on a single perishable crop. Radiation processing is used to delay ripening and extend the period during which the scopes may be brought to the market-place.

A wide range of radiation sources is used in the processing industry, such as gamma sources, electron accelerators, etc. For further reading, see the bi-annual proceedings of the International Radiation Processing Symposium (RPC 1990).

2.2.5. THE WEAPONS ENVIRONMENT

A nuclear weapon based on fission is constructed with a configuration of fissionable material slightly below the critical point. A nuclear detonation is triggered when the configuration is made supercritical. This may be achieved either by driving two pieces of subcritical material together or by imploding a spherical shell of material. The energy associated with a nuclear weapon requires a special classification scheme. Nuclear yields are expressed in equivalent kilotons (kt) or megatons (Mt) of TNT explosive. 1 kt TNT generates 10¹² cal, which should be compared with the requirement of only 56 g of U-235 to release the same amount of energy. In less than 1 μ s the detonation energy of a weapon has escaped into an air mass many hundreds of times larger than the mass of the device itself.

The energy from the weapon is transferred by four mechanisms: thermal (fire ball), blast, nuclear radiation, and electromagnetic pulse (EMP). The thermal and blast components are independent of the weapon construction; the radiation and the EMP component are determined by the weapon construction and materials and are independent of the external environment. The energy partition of a typical weapon detonated in the atmosphere is:

- Blast/shock 50 percent
- Thermal radiation 35 percent
- Delayed nuclear radiation 10 percent
- Prompt nuclear radiation 5 percent

The time division between prompt and delayed radiation is taken as 1 minute.

The radiation consists of neutrons, X-rays, gamma rays, alpha particles, electrons and secondary particles. Some 90 percent of the neutrons generated by the fission-fusion reactions are absorbed within the bomb case. Neutron fluence is roughly proportional to yield.

The gamma rays originate from two principal sources:

- Prompt gammas generated in the first few milliseconds which come from a nucleus excited by capturing a neutron and then falling back to ground state;

- Delayed gammas generated by the decay of radioactive fission fragments. The gamma spectrum extends to 12 MeV with most of the fluence in the range up to 0.75 MeV. As with neutrons, the gammas undergo geometrical attenuation as well as exponential attenuation in materials. The gamma dose can be enhanced by the lowered density of the air during the blast.

2.2.6 HIGH-ENERGY PHYSICS ACCELERATORS

Current high-energy physics research is carried out with beams of electrons or protons having very high energies, often operated so that the two beams collide and produce short-lived particles of interest in determining subatomic structure. For example, the Large Hadron Collider (LHC) under construction at CERN in Geneva is a circular accelerator and consists of two adjacent 26.7 km rings in which two proton beams run in opposite directions. The proton beams will collide in four points along the circumference at a centre of mass energy of 14 TeV. Many magnets and RF power sources are used to guide and accelerate the beam, and the target areas are surrounded by very large arrays of radiation detectors of the most advanced type, including high-speed, ultra-sensitive electronic detection circuitry. At high luminosity the proton-proton collisions at the LHC will produce an extremely hostile radiation environment. Many simulations have been performed in order to obtain realistic expectations. The total dose contribution is mainly due to the primary flux of particles coming from the interaction region. The secondary radiation that escapes from the accelerator tube consists mainly of photons and neutrons of high energy. The dose rates are of the order of $10^5 \text{Gy}(\text{SiO}_2)$ per year. The consequences for some parts and materials to withstand $10^6 \text{Gy}(\text{SiO}_2)$ opens up a new range of requirements generally higher than those needed in space radiation or the military environments.

CHAPTER 3

RADIATION HARDENED BY DESIGN (RHBD)

3.1. INTRODUCTION

To reduce radiation-induced soft errors in SRAMs, different approaches have been proposed, and they can be categorized into two types as Radiation Hardened

by Process (RHBP) approach and Radiation Hardened by Design (RHBD) approach. RHBP requires manufacturing variations away from and the standard mainstream process, i.e. the Complementary Metal Oxide Semiconductor (CMOS) process, and therefore it is expensive to be implemented. On the other hand, RHBD is easier to implement, and is favorable in research and industries for various applications.

3.2. CURRENT RHBD APPROACHES

Error Correction Code (ECC) can be loosely categorized as RHBD. It is the most popular approach to reduce the soft error rate for SRAM because of the regular nature of the memory array [19]-[21]. Through adding more bits in a word, the soft errors in single or multiple bits can be corrected by ECC, and the protection abilities of different ECCs (amount of errors can be corrected) depend on different specific algorithms. As a systemlevel hardening approach, ECC commonly involves less custom-design tasks which relatively ease the implementations. However, ECC can increase the access time of SRAM and therefore slow down the performance of the whole system.

Circuit duplication (including “Triple Module Redundancy” and “Built-in SoftError Resilience (BiSER)”) with the combination of a voting circuitry is another RHBD approach that addresses soft error problem, but this technique generates undesirable power and area overhead. Additionally, current versions of this technique cannot handle Multi-bit Upsets (MBUs).

3.3. RHBD SRAM BITCELLS

Many radiation hardened SRAM bitcell structures have been proposed, among which Dual Interlock Storage Cell (DICE) [22] and Quatro cell [23] are most favorable. A lot of researches [24]-[27] have been conducted on these structures. A DICE bitcell has twelve transistors and consumes almost twice as much area as a traditional 6T bitcell. It is, however, very effective in correcting SEU when radiation only affects one node in the bitcell. As technology continues to advance, Quatro cells exhibit better soft error resilience than DICE bitcells, especially when LET is very high. In [27], it is reported that Quatro cell exhibits better soft error rate than DICE cell in 40 nm technology.

3.4. SINGLE-EVENT EFFECTS

The passage of a single particle through a CMOS device can create a high-density ionization track, which results in charge collection in a localized region of the circuit. The upsets caused by single-event effects (SEE) can be divided into two categories, soft upsets and hard upsets.

3.5. SOFT UPSETS

A soft upset occurs when a transient pulse or bit-flip in the device causes an upset detectable at the device output. Soft upsets are entirely device specific, and are best categorized by their impact on the device.

3.6. SINGLE-EVENT UPSET

A single-event upset (SEU) occurs when the charge transferred as a result of the generated short pulse of currents is of sufficient magnitude to alter the logic state of a sensitive node. A sensitive node is a node that can collect charge on it when hit by a particle. A single charged particle can traverse through a transistor's reverse-biased p-n junction and create an ionizing path along its line of trajectory. However, the electric field across the junction is distorted along the ionizing path (this is called funneling), which increases the electric field's ability to attract the charge to one of the nodes. Taking the funneling phenomenon into consideration, more charge would be collected at the stuck node and less at the surrounding nodes. If the charge collected at the node were within the indicated range, an upset would occur. The minimum charge, which must be deposited in a device to cause an upset, is called the Critical Charge.

An upset node may further cause the alteration of the contents of circuit memory elements or alter the operation of the circuit in such a way as to cause an upset in the logic function. In the case of a static RAM cell (SRAM), which is made of two inverters in which the output of each inverter is connected to the input of the other one, the sensitive nodes are the transistors' drains. This kind of problem is of special concern in digital circuits and can be eliminated by rewriting the information lost in the case of a memory or repeating the algorithm being executed in the case of a CPU. The number of soft upsets is normally specified in upsets/bit-day. If the upset rate is too high this can lead to a significant reduction in the circuit performance.

A SRAM stores information in a latch. For an SEU to occur, the induced perturbation must exceed the charge restoration capability of the cross-coupled inverter. By a similar argument, the cell can be hardened against SEU by protecting the charge at one inverter's gate. For CMOS SRAMs that have very low static power consumption, the critical charge provides a valid measure of SEU susceptibility. The duration of the charge collection from a SEU is short compared to the write time of the SRAM cell.

3.7. SINGLE-EVENT FUNCTIONAL INTERRUPT

Single-event functional interrupt (SEFI) can be thought of as a special case of SEU. In complex memories, the memory cells and the peripheral circuits of a memory are connected to other circuits. If an energetic particle strikes one of these circuits, the upset will influence the functioning of the whole circuit.

3.8. MULTIPLE-BIT UPSET

Multiple-bit upset (MBU) is analogous to the SEU, but more than one node is affected at the same time. There are three different kinds of upsets; the first two are caused by a single particle, the third by two independent particles. In the first case a single particle strikes the integrated circuit nearly right angle of the surface, crossing in this way the sensitive volume of more adjacent devices at the same time. In the second case the particle strikes the node almost perpendicularly but deposits enough energy to be able to change the information contained in more than one sensitive node. As the feature size is reduced, MBU will be more and more common in VLSI circuits. In the third case two particles hit two nodes simultaneously, modifying their states and, in some cases, also in other devices.

3.9. HARD UPSETS

Hard upsets can be physically destructive to the device and cause permanent functional errors.

3.10. SINGLE-EVENT LATCH-UP

For CMOS circuits containing both NMOS and PMOS transistors on a silicon substrate, parasitic bipolar p-n-p-n devices exist and forms a silicon-controlled rectifier (SCR) structure, which under normal conditions is in its "off" (i.e. high-impedance) state. If a radiation induced current produces sufficient bias to turn

on one of the parasitic base emitter junctions, the SCR can be triggered, producing a low-impedance path between the power supply and ground rails. If the product of the effective current gain of the parasitic p-n-p and n-p-n devices is greater than unity, then a self-sustaining SCR high current mode is triggered. This condition is known as single-event latch-up (SEL). The SEL phenomenon is similar to the electro-static discharge induced latch-up protected against in typical CMOS I/O structures, however in an ionizing radiation environment, a particle can strike anywhere in the circuit so merely protecting the I/O circuitry is not sufficient. SEL is a potentially destructive condition. During a traditional or destructive SEL, the device current exceeds the maximum specified for the device. Unless power is removed, the device will eventually be destroyed.

3.11. SINGLE HARD ERROR

If a particle crosses the gate oxide layer of an MOS transistor, it may deposit a sufficiently large total dose to induce a threshold voltage shift, which results in a failure of the device. This phenomenon is called single hard error (SHE). SHE causes a permanent change to the operation of the device. A common example would be a stuck bit in a memory device. Like SEUs, this is also device dependent. For example, in a DRAM cell, the sub-threshold current of the pass transistors can become high enough to conduct the charge on the storage capacitor to the word line all the time, and no information can be stored in the cell.

3.12. SINGLE-EVENT GATE RUPTURE

Single-event gate rupture (SEGR) is an irreversible event that consists of the destruction of the gate oxide by an ionizing particle. This problem is especially important in the situation where there is a high electric field on the gate oxide, as for example during the writing or erasing phase of EEPROM (Electrically Erasable Programmable Read-only Memory) or in power MOSFET devices.

3.13. SINGLE-EVENT BURN OUT

Single-event burn out (SEBO) is present in power MOSFET's and bipolar transistors, since these devices contain a parasitic bipolar transistor. In some biasing conditions it is possible that an ionizing particle turns on the bipolar transistor, and if this is able to conduct enough current the locally power can be high enough to melt the entire transistor.

3.14. SUMMARY

There are three primary types of radiation effects:

- Total dose effects results from the interaction of ionizing radiation with silicon oxide, generating charge or charged centers which change device properties. These effects depend upon the total ionizing energy absorbed in the material (the total dose);
- Single-event effects results from the interaction of a single energetic particle passing through a device. Historically these effects have been associated with the high density charge track created by the particle;
- Displacement damage effects results from the displacement or dislodging of atoms from their normal sites in a crystal lattice or material structure due to the nuclear interaction of energetic particles. These interactions create defect sites in the material. MOSFETs are not sensitive to this type of effects, as a MOSFET is using majority carriers instead of minority ones, which are effected by displacement damage effects.

CHAPTER 4

EXISTING SRAM BITCELL DESIGNS

4.1. INTRODUCTION

Overall the years, many different designs have been proposed for SRAM bitcell structures. This Chapter introduces several SRAM bitcells that are used in both industry and academic research. Section 4.2 introduces the 6T bitcell, which is most commonly used in the industry because of its compact size. Section 4.3 introduces DICE bitcell and section 4.4 introduces Quatro bitcell, and their single event upset correction mechanism is also analyzed.

4.2. 6T SRAM BITCELL

In microelectronics, a cross-coupled inverter pair is the foundation of the static storage elements, including SRAMs, register files, latches and flip-flops. The crossed-coupled inverter can constantly refresh its logic through a strong positive feedback using two inverter pairs. The most popular and widely implemented structure in commercial SRAMs is the conventional 6-Transistor (6T) structure

as shown in Figure 4.1 (a) (b). As shown in the Figure 4.1 (a), the 6T cell contains a pair of cross-coupled inverters (P1, N1 and P2, N2), which can hold the states, and a pair of access transistors (N3 and N4), which are used to read/write the state from/into the nodes. Two internal nodes Q and QB are used to store logics. Two inverter pairs P1, N1 and P2, N2 have positive feedback on each other to constantly refresh logic. Two access transistors A1, A2 are controlled by WL signal and they connect Q, QB to BL, BLB.

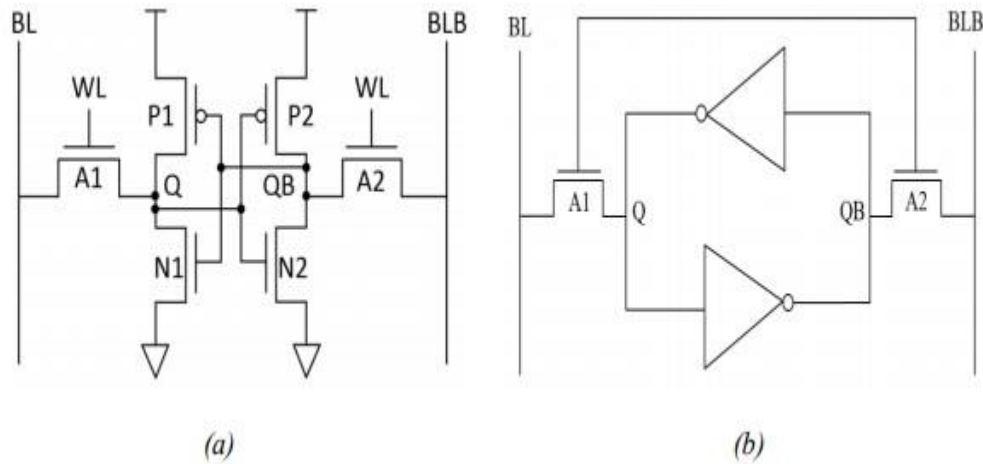


Figure 4.1 (a) Schematic of traditional 6T SRAM bitcell (b) 6T bitcell composed of two back-to-back inverters and two access transistors A1, A2

In read operation, BL and BLB are first pre-charged to high. WL is activated and then A1, A2 are turned on. The BL or BLB starts to be pulled down depending on what logic stores in Q and QB. In order to pull down the voltage in BL/BLB, the size of N1, N2 needs to be bigger than A1, A2 to make sure that the original logic will not be corrupted in the cell. In general, $(WN1/LN1)/(WA1/LA1)$ or $(WN2/LN2)/(WA2/LA2)$ (bitcell ratio) can vary from 1.25 to 2.5 in various applications [34]. The voltage difference developed in BL and BLB will overcome the offset of the sense amplifier, which will swing the output to be a complete digital logic.

In write operation, the data will first be loaded in BL and BLB. After WL is turned on, the data starts to write into Q and QB. In order to guarantee a successful write operation, the access transistor should have a bigger drivability than the pull-up transistors P1, P2. In general, a successful write operation can be guaranteed by choosing the $(WA1/LA1)/(WP1/LP1)$ or $(WA2/LA2)/(WP2/LP2)$ (pull-up ratio) less than or equal to 1.

As indicated in [15], there are two important aspects in SRAM design, one is cell size and the other is the stability. For the size, the 6T bitcell has the least area penalty and therefore is very favorable in many applications in the industry. But for the stability, the 6T design is very vulnerable to radiation strike. Once one of the two internal nodes is flipped by radiation, the positive feedback can easily flip the content of the whole cell.

Static Noise Margin (SNM) is defined as the maximum static spurious noise that a bitcell can tolerate while still maintaining a reliable operation. SNM is a very important design metric and a good design should have sufficient SNM to withstand dynamic noise from different sources, such as coupling, soft errors, supply voltage fluctuations, and change in voltage dependent capacitances in the bitcells.

4.3. DUAL INTERLOCK STORAGE CELL

A dual interlock storage cell (DICE) consists of eight interlocked inverters and four access transistors as shown in Figure 4.2, and is first proposed in [22]. Unlike traditional 6T cells, four internal nodes A, B, C, D are used to store logics, instead of two nodes. The two logic states stored in the cell are either “1, 0, 1, 0” or “0, 1, 0, 1”. So by using redundant nodes to store logic, DICE is a lot more robust than the traditional 6T cell. Many previously proposed designs [24] [25] [36] are all based on DICE.

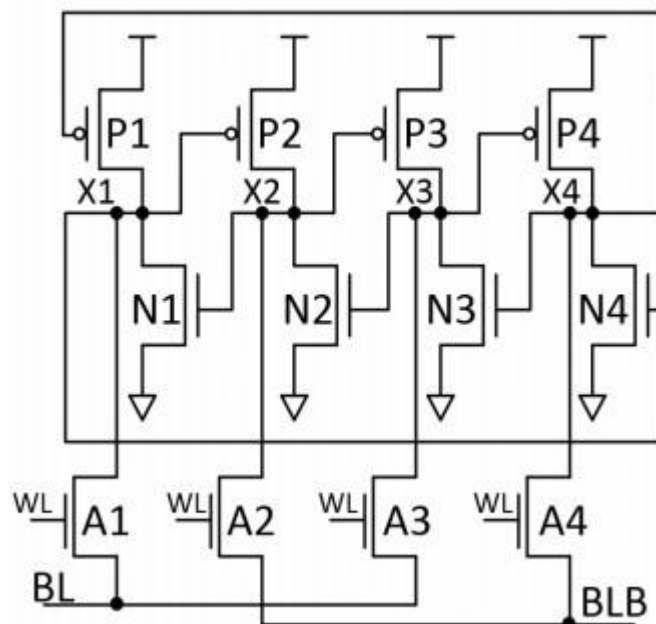


Figure 4.2 Schematic of DICE bitcell

The fundamentals of SEU recovery mechanism of DICE is explained as followed. Suppose the original logic 0, 1, 0, 1 is stored in the cell, and a ray of radiation is striking N2 which pulls the voltage of node X2 from 1 to 0. In this case, node X2 turns off N1 and turns on P3. Therefore, P3, N3 are both turned on at the same time in this moment, but node X3 can maintain a relatively low voltage and the logic is not affected (pull-down NMOS has stronger drivability than pull-up PMOS in memory design). Both P1 and N1 are turned off at this moment, X1 is kept floating and can be maintained at a very low voltage; therefore the logic is considered not affected. Eventually after the SET is gone, X2 can recover back to 1. Figure 2.3 shows the recovery waveform [22]. As can be seen from the waveform, node X2 is pulled down completely from 1 to 0, but the voltage of node X3 only rises up a bit and doesn't change its logic. Eventually node X1 recovers back to 1, and X3 also goes back to 0 completely.

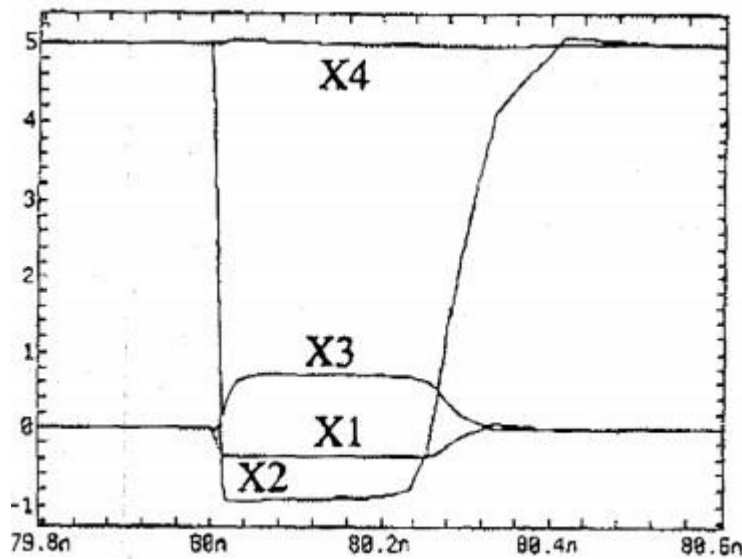


Figure 4.3.1 Recovery waveform of logic when X2 is flipped from 1 to 0

In the same logic when X1, X2, X3, X4 are still 0, 1, 0, 1, when radiation strike P1 and flip X1 from 0 to 1, the recovery mechanism is as follows. In this case, X1 is flipped from 0 to 1, so node X1 will turn on N4 and turn off N2. Node D will actually be changed to 0 (in memory design pull-down, NMOS has stronger drivability than pull-up PMOS). For node X2, because N2 and P2 are both turned off, it is floating and therefore considered as unaffected. So X1 and X4 are affected, but X2 and X3 are unaffected. As N1 is kept turned on by node X2, after

the SET is gone, X1 can recover back to low voltage. As soon as X recovers, X4 recovers back to 1. The following Figure 2.4 shows the recovery waveform. As shown in the figure, X1 recovers back to 0 at around 75.3 ns, and X4 recovers at around 75.4 ns.

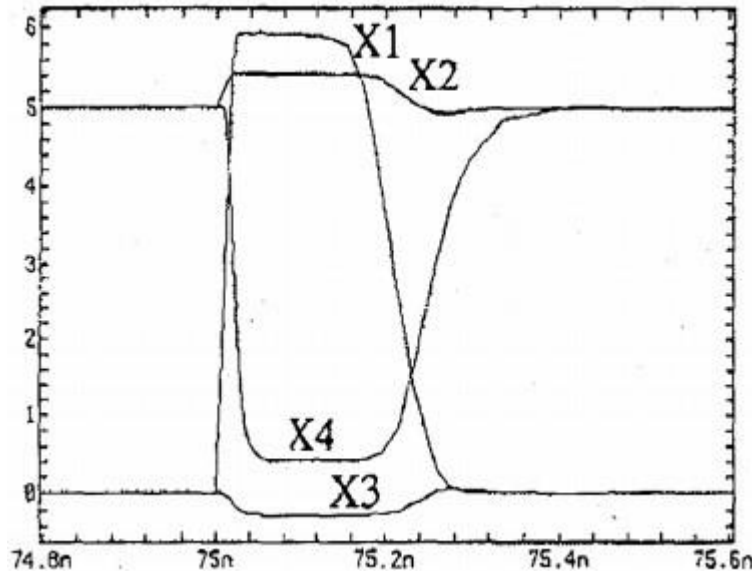


Figure 4.3.2 Recovery waveform of logic when X1 is flipped from 0 to 1

In legacy technologies, DICE cell has been proven to be very effective in mitigating soft errors. In the sub-100 nm technology, however, DICE is not as superior as traditional design because the radiation can affect several nodes simultaneously due to shrinking device dimension. It has been verified that at 40 nm technology, DICE-FF exhibits only 1.4X improvement over the DFF in neutron and proton environments [37]. It is reported that DICE has a total of 6 sensitive node pairs, and another RHBD bitcell called Quatro [23] has sensitive node pairs of 4 [27]. It has been reported that Quatro bitcell exhibits a better soft error rate than DICE cell in 40 nm technology.

4.4. QUATRO 10T SRAM CELL

Quatro cell is initially proposed in [23], and it is composed of ten transistors, as shown in Figure 4.4. This cell also has four internal nodes (A, B, C, D). Unlike the DICE cell where the four internal nodes are dual interlocked, the four nodes in Quatro cell are in a CVSL (Cascode Voltage Switch Logic) logic. Quatro cell only uses ten transistors and has less area overhead compared to DICE bitcell.

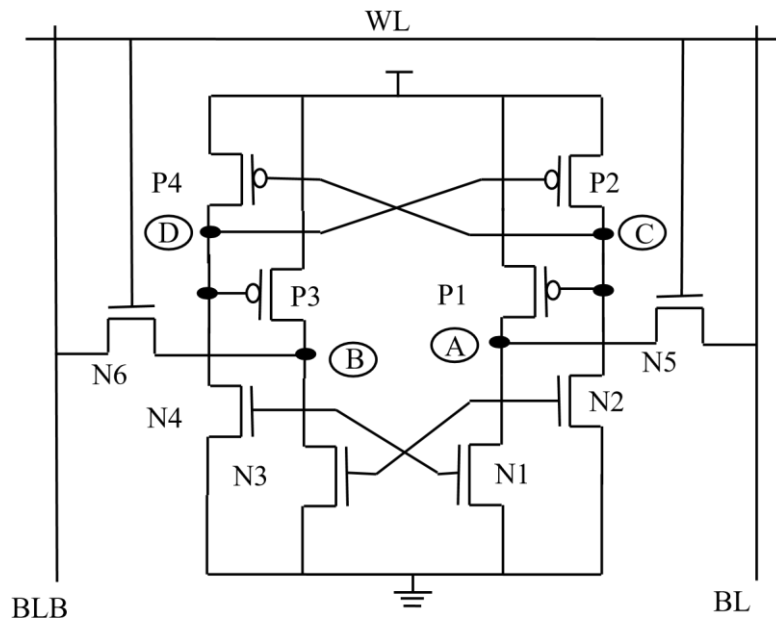


Figure 4.4 Schematic of Quatro-10T bitcell

Quatro cell also has soft error correction capability. Supposing the logic state stores in A, B, C, D are 1, 0, 1, 0 respectively, if a ray of radiation strikes N1 and pulls node A down to logic 0, N2 and N3 will be turned off, so node B and C are floating. The voltage of B and C can be kept at 1, so after the transient is gone, node A can recover back to 0 because N1 is kept turned on by node B and P1 is kept turned off by node C. Figure 4.4.1 shows recovery waveform after node A is flipped from 1 to 0. Node B, C, and D are basically not affected, and node A recovers back to voltage 1 at about 200 ps.

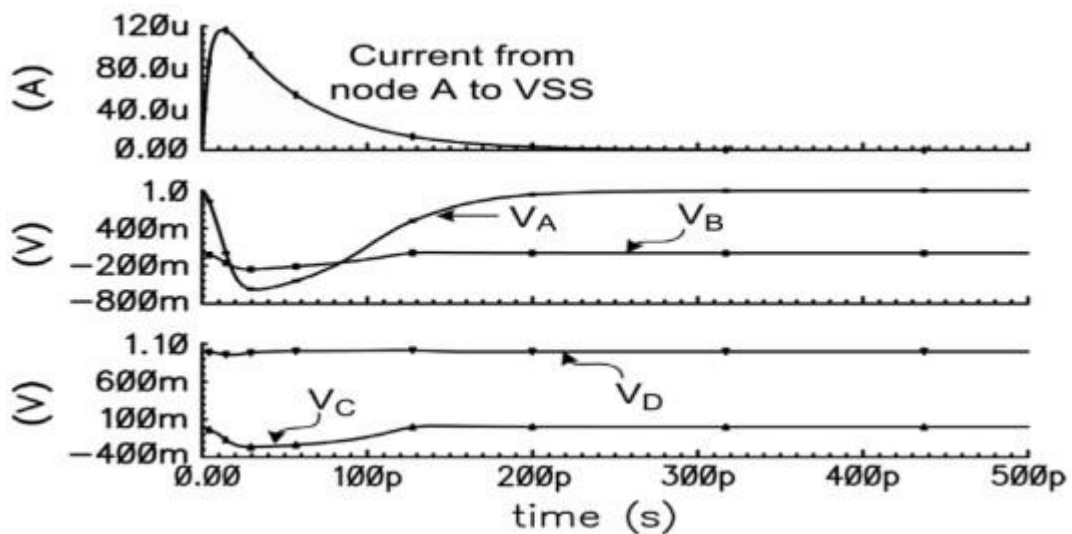


Figure 4.4.1 Quatro cell recover when Node A is flipped from 1 to 0

There are scenarios when Quatro cell is sensitive to SEU. For instance, when the logic stores in A, B, C, D are 0, 1, 0, 1, if a ray of radiation strikes P1 and flips the voltage from 0 to 1, node A consequently turns on N2 and N3, so N2 and N3 are able to pull node A and C down to very low voltage (pull-down NMOS has higher drivability than pull-up PMOS in SRAM bitcell). Therefore, nodes A, B, C are flipped, and the cell's logic will be flipped. As long as three nodes are flipped in a cell, the cell is not able to recover. Figure 4.4.2 shows the flipping waveform. In Quatro bitcell there are two nodes that are sensitive to SEU. When the logic state is 0, 1, 0, 1, node A is sensitive to 0 -> 1 upset. When the logic state is 1, 0, 1, 0, node B is sensitive to 0 -> 1 upset.

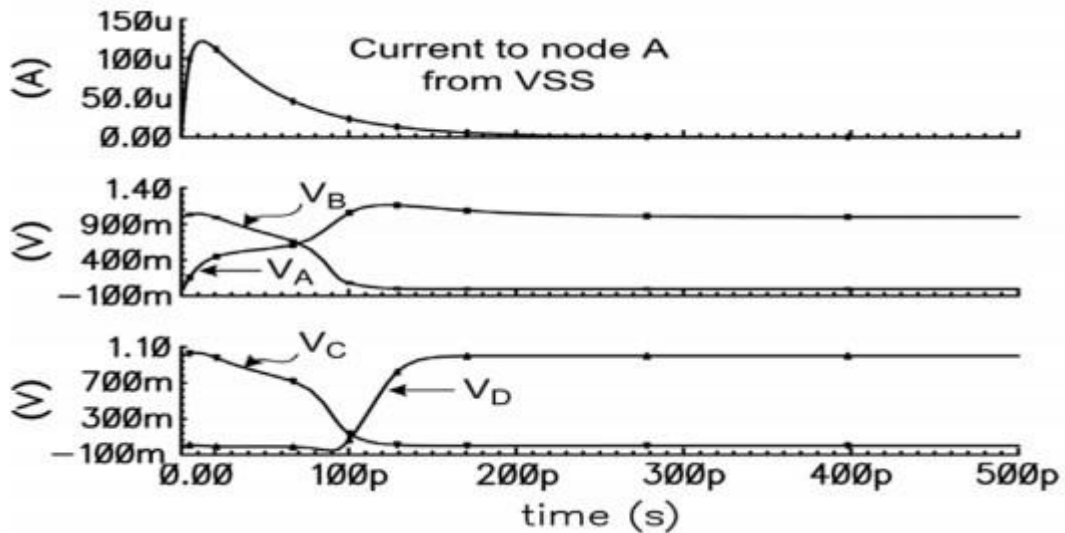


Figure 4.4.2 Quatro cell is upset because Node A is flipped from 0 to 1

CHAPTER 5

PROPOSED CELL, OPERATIONS AND RESULT

5.1 INTRODUCTION

The Aerospace market in India is estimated to reach around \$70 billion by 2030. One of the major components used in it is memory. SRAM cell is used for cache memory, which occupies 90% of the chip area. The smallest transistors that are sensitive to process variations are used. The PVT (Process, Voltage, Temperature) variations affect the device threshold voltage (V_t) which in turn modifies the drain to source current (I_{DS}) [1]. SRAM cells consume power for data retention in standby mode because of various leakage current components. With the minimization of the technology, the memory cells of SRAM (Static Random Access Memory) are more susceptible to radiation particles, like alpha particles, heavy ion and cosmic rays because they have lower supply voltage and smaller node capacitance. Less signal charge and decreased noise margin makes the Nano scale integrated circuits extremely susceptible to particle-induced single event transients (SETs) [2]-[3]. Packaging materials and intergalactic rays produce alpha particle and cosmic neutrons which cause SETs. These particles generate extra charge through direct or indirect ionization in silicon, which are collected by sensitive nodes and they create voltage transients at those nodes [4].

A cross-coupled inverter pair is regarded to be a latch. The large value of the transient's amplitude and duration alters the value stored in the latch which in turn results in a single event upset (SEU). As the damage caused to the device by a SEU is not permanent, it is called as a 'soft error'. This soft error can cause the state of SRAM to be disturbed and can lead to the malfunctions of the system [5]. The radiation particles passing through the sensitive nodes of SRAM cell release Electron-hole pairs along the paths of these sensitive nodes. Under the action of the electric field, holes travel towards the source region of the transistor, and the electrons move towards the drain end of the transistor. Electrons accumulated to a certain extent changes the stored state in this sensitive node. In order to limit the SRAM SER, Error correction codes (ECC) or soft error hardened memory cells are used.

Three types of failures are common in SRAM cell [6] –hard failures, soft failures and parametric failures. 1) Open or short conditions cause hard failures. 2) Soft failures are caused by three major sources. The radioactive impurities such as packaging materials releases alpha particles, terrestrial cosmic radiations release high-energy neutrons and thermal neutrons are released by the interaction of the cosmic ray [7]. 3) Parametric failures are caused by variation in the design parameters. Abrupt increase in SRAM cell access time causes access failure which is included in parametric failures; Read failure is caused by flipping of cell state while reading; Write failure is due to the lack of capability to write to a cell and hold failure is caused by the standby mode flipping of the cell content, primarily when V_{DD} approaches or falls below DRV (data retention voltage). In this paper, we proposed a 10T radiation hardened SRAM cell with PMOS access transistors that is radiation hardened when compared with Quatro 10T SRAM cell.

5.2. PRIOR WORK

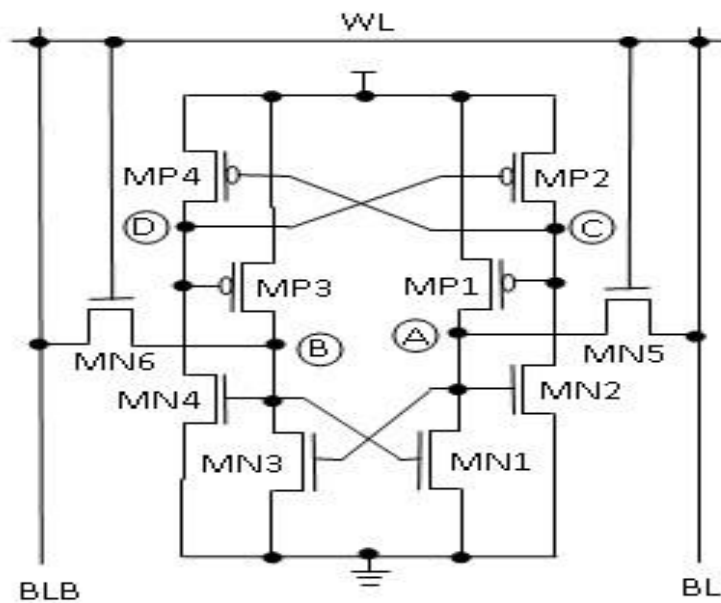


Fig.5.1. Schematic of Quatro-10T SRAM cell

The basic Quatro-10T SRAM cell shown in Fig.5.1 in which four PMOS transistors (MP1, MP2, MP3 and MP4), four NMOS transistors (MN1, MN2, MN3 and MN4) and two NMOS access transistors (MN5 and MN6) connected with two bitlines (BL and BLB) to the storage nodes A and B are present [8]. If

the stored bit at node A is assumed to be at logic '0', then the logic values at nodes B, C, and D are '1', '1' and '0', respectively. Access transistors MN5 and MN6 are cutoff to show how the storage nodes maintain the same logic values when the circuit is in HOLD mode. Storage node A is having a logic value of '0', because the path of charging to VDD by the MP1 is cutoff and the path to discharge to ground by the MN1 is available. This implies that PMOS transistor MP1 is OFF and NMOS transistor MN1 is ON. Gate of MN1 is connected to node B. Since the logic value at node B is maintained at '1', it switches MN1 ON which allows node A to have path to discharge to logic '0'. Since node B is at logic '1', MN4 is ON pulling node D down to logic '0', which turns MP2 ON, raising node C to logic '1'. Gate of MP1 is connected to node C. Hence, the logic value at node C is maintained at '1' to cutoff MP1. As the storage node C is at logic '1', and then the PMOS transistor MP4 will be OFF as the gate is connected to the storage node C. This removes the path of charging to VDD for node D. MN4 is ON, as the gate is connected to storage node B which is having a logic value of '1'. Hence the node D will discharge to '0' since it has a path to discharge to ground.

This cell is designed in such a way to get back to these values in any case. If the stored bit at node A is at logic '1', then the logic values at nodes B, C, and D are '0', '0' and '1', respectively. This also is maintained in the similar fashion by the switching action of the PMOS and NMOS transistors connected to the nodes. When the node voltage is pulled down (up) by a SET, 'ON' PMOS (NMOS) transistor connected to the node restores the node voltage and unaffected node drives it. If PMOS (NMOS) transistor is turned on by SET, to pull up (down) its drain voltage the transistor has to work against an unaffected 'ON' NMOS (PMOS) transistor. Thus, an accidental flipping of the cell is prevented by a negative feedback. If multiple nodes are simultaneously affected by a SET through charge sharing [9], the proposed Quatro-10T cell may flip like the DICE cell [10]-[11]. The location, magnitude, and duration of the transients are the main causes of such a failure. When two nodes of the same potential (nodes A and D or nodes B and C) are affected this leads to the worst case.

Therefore, the Quatro-10T is laid out by keeping the "same potential nodes" as physically apart as possible to reduce the possibility of upsets due to charge sharing.

5.3 PROPOSED 10T SRAM CELL

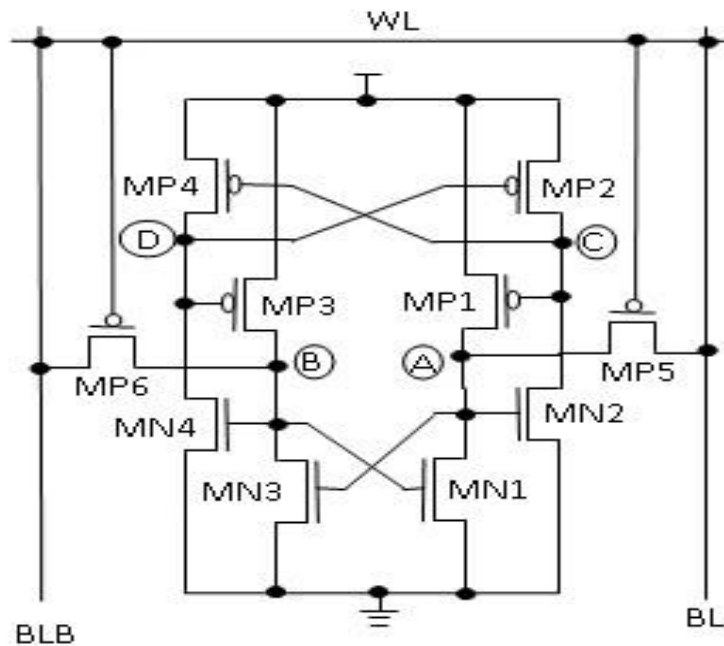


Fig.5.2. Schematic of proposed 10T SRAM cell with PMOS access transistors

This paper proposes a radiation hardened 10T SRAM cell. As shown in Fig. 5.2 it has four PMOS transistors (MP1, MP2, MP3 and MP4), four NMOS transistors (MN1, MN2, MN3 and MN4) and 2 PMOS access transistors (MN5 and MN6) connected with two bit lines (BL and BLB) to the storage nodes A and B. If the stored bit at node A is at logic '0', then the logic values at nodes B, C, and D are '1', '1' and '0', respectively. The restoring of logic values at nodes happens in a similar way to the Quatro cell. To get the benefit of higher radiation tolerance PMOS transistors are used as major devices. After radiation bombardment, leakage current increases in NMOS transistors but remains almost unaffected in PMOS devices. The stored data in storage node of the cell can get corrupted by the excessive leakage in access transistor. Therefore, the hold failure probability of the SRAM cell is improved by the usage of PMOS transistors. Moreover, gate leakage of PMOS devices has an order of magnitude smaller than NMOS transistors [6].

5.4 CELL SIZING

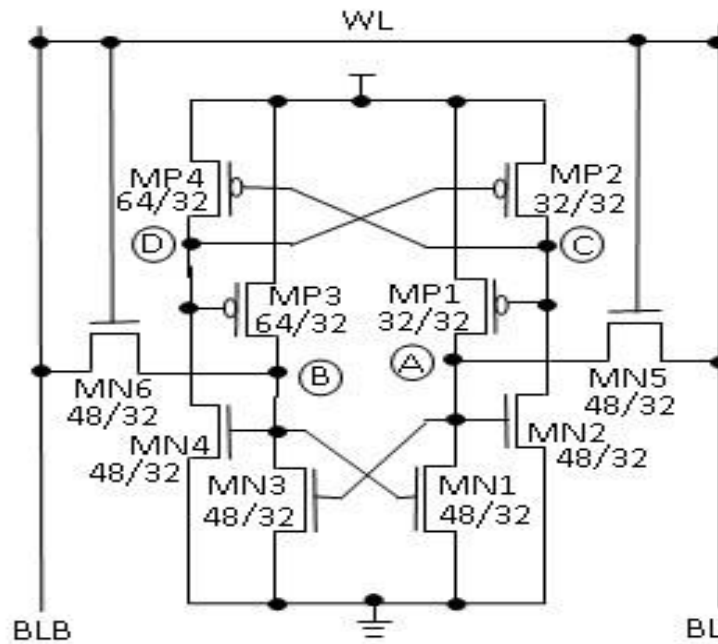


Fig.5.3. Cell Sizing of the Quatro 10T SRAM cell (all the W/L dimensions of the MOSFETs are in nanometers)

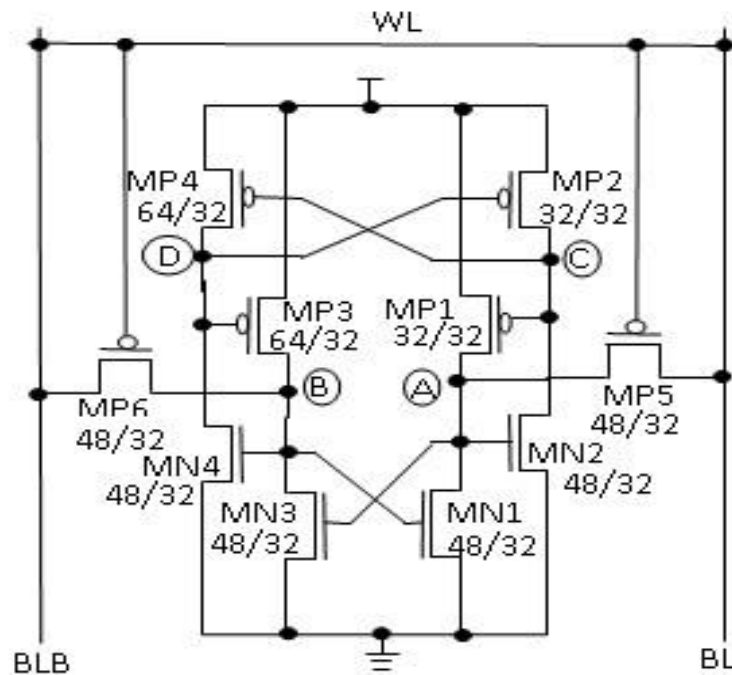


Fig.5.4. Cell Sizing of the proposed 10T SRAM cell (all the W/L dimensions of the MOSFETs are in nanometers)

The sizes of the transistors in 10-T cell and other parameters must be taken into account such that during read operation the information present in the cell should not be destroyed and modification of data should be allowed in write operation. Above two requirements must be satisfied to get the aspect ratio (W/L) of

transistors. The cell sizing of Quatro 10T as shown in Fig. 5.3 is done keeping in mind the Static Noise Margin (SNM) for a stable read operation. For the case of read operation the word line (WL) is made high to turn ON the access transistors MN5 and MN6. The BL (BLB) is discharged by the pulldown transistor MN1 (MN3) in the case when $V_A = 0$ (1). This gives us a differential bit line voltage. This helps us in achieving reliable sensing in the case of worst-case bit line leakage.

The static noise margin is affected by the aspect ratio of MN5 and MN1 or (MN6 and MN3). The cell ratio (CR) should be in the range of 1.5 to 1.7 [12]. CR is defined as the ratio of (width/length) of MN1 and (width/length) of MN5 i.e. $(W_{N1}/L_{N1})/(W_{N5}/L_{N5})$ [13]. The cell sizing of MN1 and MN5 is done according to the cell ratio. In the case of read operation, the value stored at node A is assumed to be 0. If the cell is affected by SET it may get changed to 1. So, MN1 and MN5 should be stronger than the MP1 for the restoration of the value 0 because it has a path to discharge to 0. MN1 should be stronger than MN5 to obtain a better value of RSNM at node A. MN5 should be stronger than MP1 for obtaining a better write ability.

Similarly, the value stored at B is assumed to be 1. When it gets affected by SET it gets changed to 0. So, the value of MP3 should be stronger than MN3 for the restoration of 1 because it has a path to get charged to V_{DD} . Similarly, to maintain the configuration of the stable read operation we have taken cell ratio as shown in the Fig. 5.3. This cell sizing helps in retaining the stored values even if a SET affects it. Therefore, W/L ratio for the transistor MN1, MN2, MN3, MN4 is (48/32), for MP1 and MP2 is (32/32), for MP3 and MN4 is (64/32), for MN5 and MN6 is (48/32). In the case of proposed 10T cell as shown in Fig. 5.4 for a stable read operation the process of recovering from 0 to 1 or from 1 to 0 at any node is same as the Quatro 10T. The only difference in the case of proposed cell is word line is switched OFF. Therefore, the sizing of proposed 10T cell is also done in a similar way to that of Quatro 10T. For the proposed cell W/L ratio for MP5 and MP6 is 48/32 and the rest is same for all other transistors.

5.5 OPERATIONS OF THE PROPOSED 10T CELL

5.5.1. READ ACCESS TIME (T_{RA})

The estimation of T_{RA} (read access time or read delay) is done from the time WL (word line) gets activated to the time when BL (bit line)/BLB (bit line bar) gets discharged by a value of 50 mV from its initial high level. The differential voltage of 50 mV between BL and BLB is good enough to get detected by the help of sense amplifier, hence avoiding misread operation [13]. The estimation of T_{RA} (read access time or read delay) is done from the time WL (word line) gets activated to the time when BL (bit line)/BLB (bit line bar) gets discharged by a value of 50 mV from its initial high level. The differential voltage of 50 mV between BL and BLB is good enough to get detected by the help of sense amplifier, hence avoiding misread operation. In the proposed 10T cell instead of activating the word line, we estimate the T_{RA} when WL is deactivated. Initially BL and BLB are pre-charged. Here, also we sense 50-mV difference between BL and BLB by sense amplifier to avoid misread [14]. The estimated T_{RA} are reported in Table I, from where it is observed that the value of T_{RA} for Quatro 10T cell is less as compared to the proposed 10T cell. In Quatro 10T cell, the access transistors are NMOS whereas in proposed 10T cell the access transistors are PMOS. The majority charge carriers in NMOS are electrons whereas the majority charge carriers in PMOS are holes. As we know that electrons are more mobile as compared to holes, it takes less read time. This explains why the T_{RA} of the proposed cell is more compared to that of Quatro 10T cell as shown in the Fig. 5.5. The Monte Carlo analysis is done with 5000 sample size and the distribution plot is shown in Fig. 5.6 for both Quatro and proposed cell. We observed a greater mean in Quatro as compared to proposed cell. The spread of the Gaussian-like curve is better for the proposed cell.

TABLE 5.1
COMPARISON OF T_{RA} VALUES FOR DIFFERENT V_{DD}

VDD	QUATRO 10T SRAM	PROPOSED 10T SRAM
0.6	2.828e-11	2.804e-11
0.65	1.955e-11	1.995e-11
0.7	1.463e-11	1.526e-11
0.75	1.155e-11	1.224e-11

0.8	9.485e-12	1.017e-11
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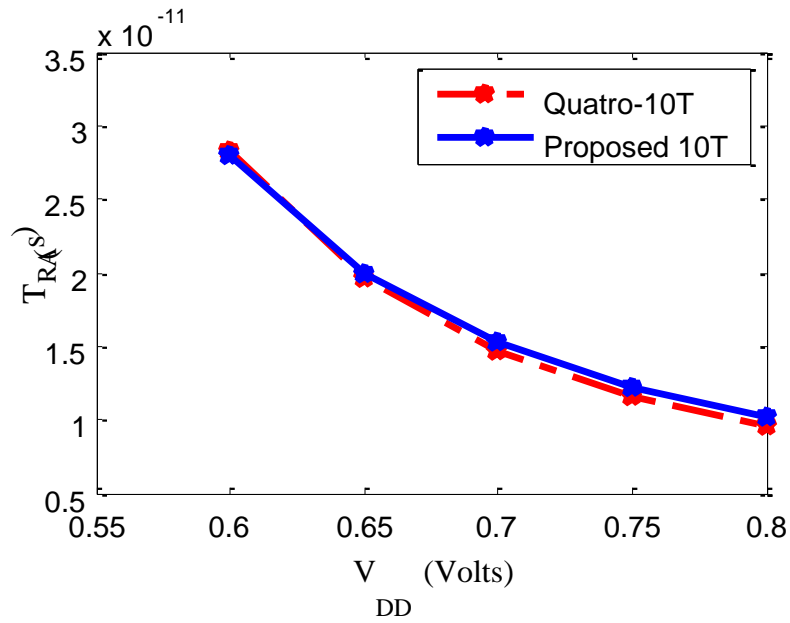


Fig.5.5. T_{RA} of Quatro 10T cell and proposed 10T cell at various V_{DD}

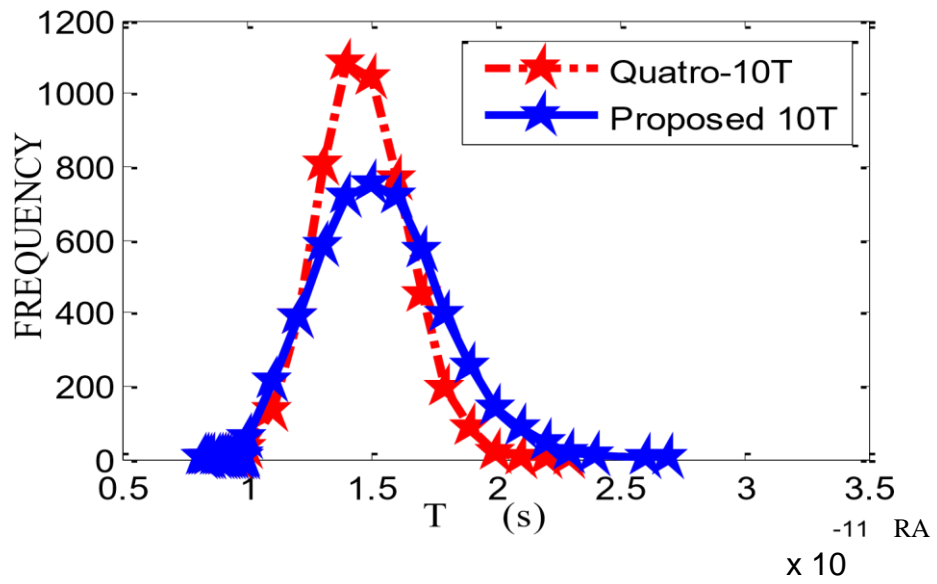


Fig.5.6. Comparison of T_{RA} distribution plots for Quatro-10T and Proposed 10T SRAM cells with sample size of 5000 while performing Monte Carlo simulation

5.5.2. HOLD POWER

When the leakage current is high, Hold operation has its own significance for data retention. For the purpose of long data retention during hold mode, word line (WL) is disabled and the BL and BLB lines are pre-charged and the partial cross coupled inverters are tightly connected to each other [16]. We measured the hold power using transient analysis by taking the readings of I_{avg} , and we calculated the hold power by multiplying the value of I_{avg} with the supply voltage. In the case of proposed cell WL is made high to cut off the access transistors for hold operation and the rest calculation remains same.

The hold power for both Quatro and proposed cell is observed to be same as shown in Table II. In the case of hold operation, the access transistors are cut off so there is no change in the operation for the Quatro and proposed cell. Hence, there is no change in the value of hold power. The Fig.5.7 shows that as we keep on increasing the values of V_{DD} the value of hold power also increases gradually. As we know that the power increases with increase in voltage the same phenomena occur here.

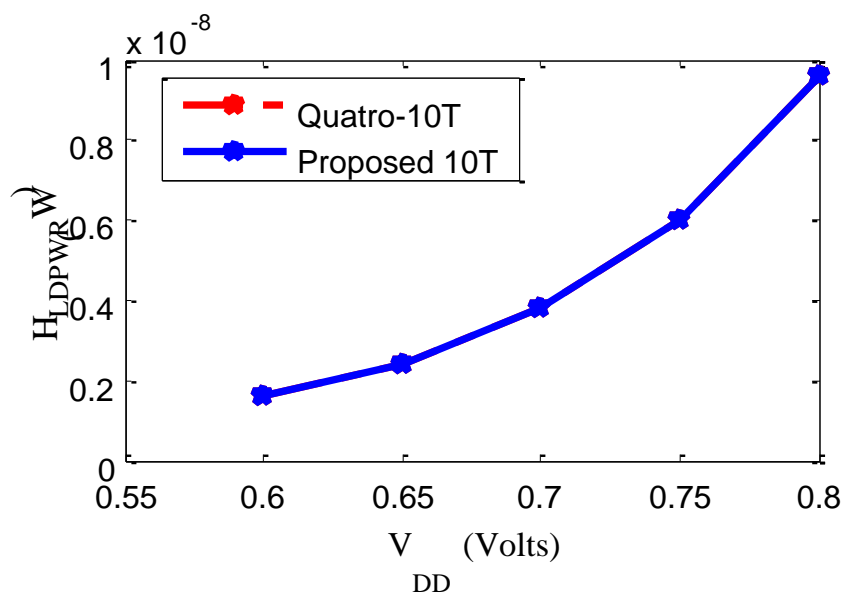


Fig.5.7. Hold Power of Quatro 10T cell and proposed 10T cell at various V_{DD}

TABLE 5.2
COMPARISON OF HOLD POWER VALUES FOR DIFFERENT V_{DD}

V_{DD}	QUATRO 10T SRAM	PROPOSED 10T SRAM
0.6	1.6e-09	1.6e-09
0.65	2.4e-09	2.4e-09

0.7	3.8e-09	3.8e-09
0.75	6.0e-09	6.0e-09
0.8	9.6e-09	9.6e-09

5.5.3. READ STATIC NOISE MARGIN (RSNM)

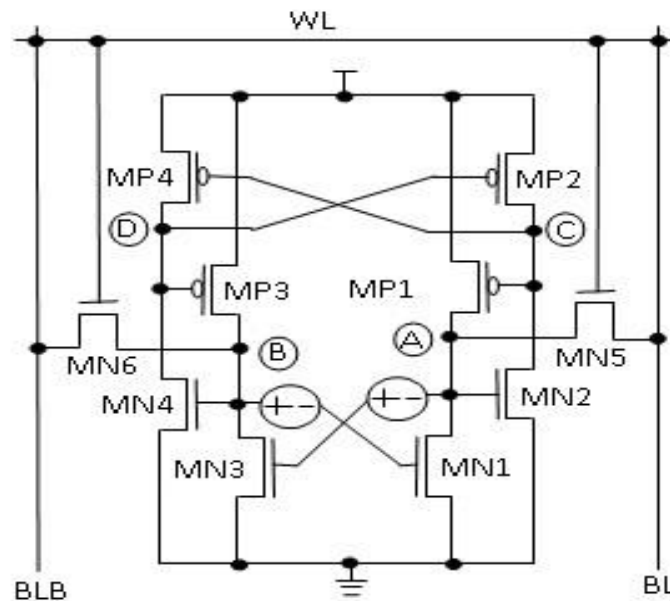


Fig.5.8. Quatro 10T cell with DC noise inserted at storage nodes A and B

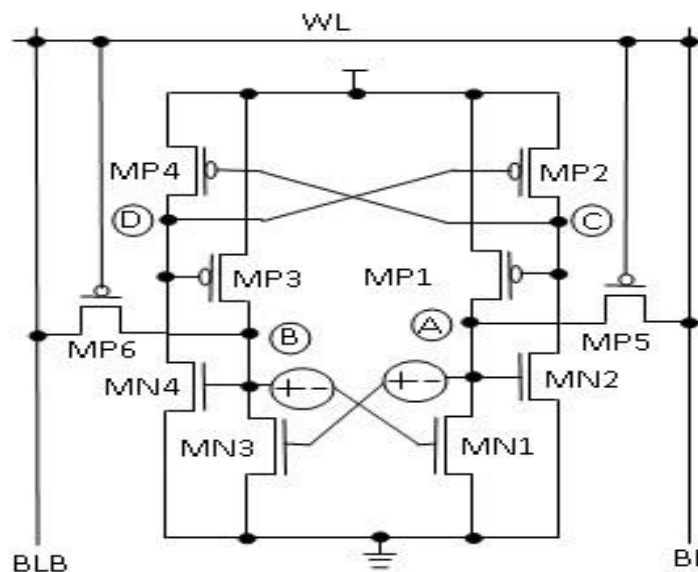


Fig.5.9. Proposed 10T cell with DC noise inserted at storage nodes A and B

The minimum DC noise voltage which is needed to flip the cell is known as Static Noise Margin (SNM) [17]. It is one of the rapidly used design parameters to measure the stability of the cell. Fig. 5.8 shows the connections needed to measure the SNM of Quatro 10T cell. Butterfly curve is used to plot the obtained results as shown in Fig. 5.10. The read stability of the SRAM cell is determined by read

static noise margin (RSNM). The length of a side of the largest square that can be inscribed inside the smaller lobe of the butterfly curve is used to estimate the noise margin. So the noise margin estimation is done in a graphical manner [18]. The following steps are followed to obtain the butterfly curve: 1) Initially both the BL and BLB are pre-charged and WL is biased at ground. 2) We insert two voltage sources N1 and N2 connected to the gates of MN3 and MN1 respectively to introduce the DC noise at all storage nodes. 3) Both the voltages of N1 and N2 are swept from 0 V to V_{DD} to calculate the measuring voltage of storage nodes A and B respectively. 4) These measured voltages are plotted which results in butterfly curve. For measuring RSNM we first measure the value of V_{bump} which is the maximum voltage of the storage node B and the RSNM is calculated.

In the case of proposed cell as shown in Fig, 5.9 all, the steps are followed in the same manner except that here WL is biased to supply voltage and BL and BLB are initially pre-charged. DC noises introduced are also the same and the rest process remains similar. We can observe from the Fig. 5.10 that the butterfly curve for both Quatro 10T and proposed 10T is obtained in similar manner. This is because, for a stable read condition the DC noises are affecting the transistors which have the capacity to drive the storage nodes but not the access transistors. So, there will be no change in the value of RSNM for both Quatro and proposed 10T cells. Therefore, both the butterfly curves overlap each other as shown in Fig. 5.10. The square is placed in the smaller lobe and RSNM value is obtained to be 222 mV.

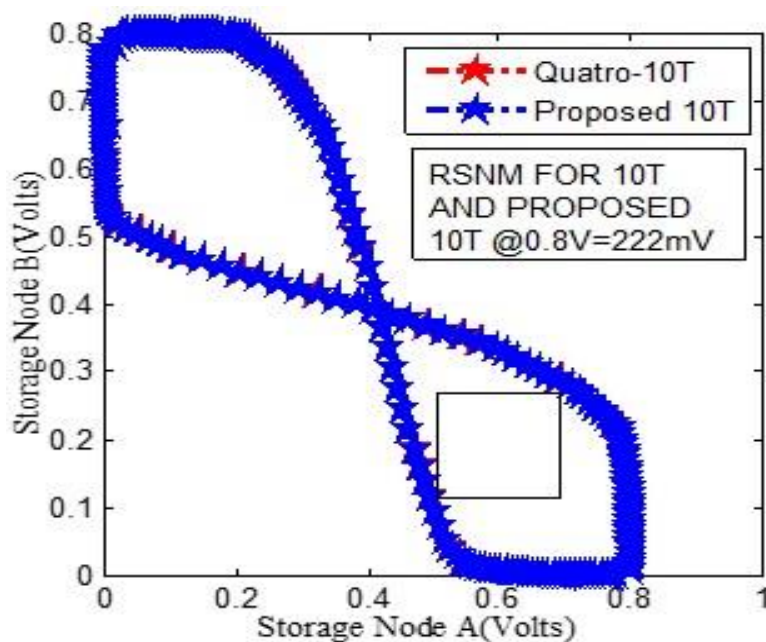


Fig.5.10. RSNM butterfly curves for Quatro 10T and proposed cell

5.5.4. WRITE STATIC NOISE MARGIN (WSNM)

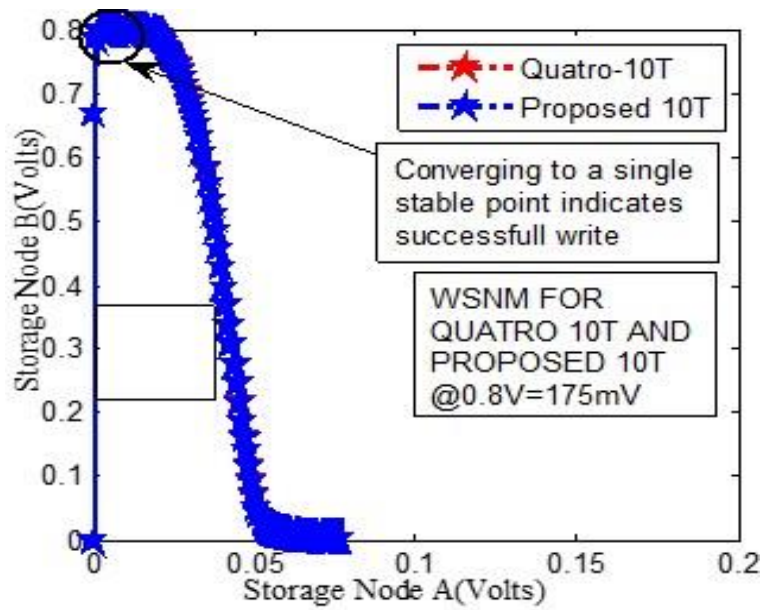


Fig.5.11. WSNM graph of Quatro and proposed 10T cell

The write static noise margin (WSNM) is a measure of the ability of the cell to pull down a node storing "1" to a voltage less than V_M (switching threshold) of the other inverter storing "0", so that flipping of the cell state occurs [12], [18].

Write-ability of a cell is measured graphically using read and write VTCs (voltage transfer curves) [12], [15]. Write VTC is measured by sweeping V_B (Fig. 11, y-axis) with BLB & WL high and BL low and monitoring V_A (Fig. 5.11, x-axis) while writing "1" to "B". This write VTC is used in combination with the read VTC, which is measured by sweeping V_A (Fig. 5.11, x-axis) and monitoring V_B (Fig. 5.11, y-axis). The side length of the smallest square, that can be embedded between the read and write VTC of the same SRAM cell at the lower half of the curves, passed the trip voltage of InvB, represents WSNM. When WSNM falls below zero, write VTC intersects read VTC, this shows positive write margin and signifies write failure [19]. The cross-coupled inverters of the cell can function as a monostable circuit because the read VTC and write VTC converges to a single stable point as shown in Fig. 5.11, which signifies a successful write operation. In the case of WSNM the Quatro 10T cell word line is biased to ground and V_{BL} and V_{BLB} are biased to ground and supply voltage respectively. For the proposed cell, the Word line (WL) is biased to supply voltage and V_{BL} and V_{BLB} are biased to ground and supply voltage respectively. The VTC curves are obtained as shown in the Fig. 5.11. We observe that the curves are over lapping for both

Quatro and proposed 10T cell, i.e., they are having same values of WSNM. This is because the access transistors are unaffected so the value of WSNM for Quatro and proposed 10T cells are same. The value of WSNM is measured by inscribing the smallest square inside the curve and the length of the side of the smallest square gives the value of WSNM [18], which is equal to 175 mV for both Quatro and proposed 10T cells.

5.5.5. SOFT ERROR ROBUSTNESS

For the Quatro and proposed 10T cell, the soft error robustness is verified by injecting an exponential current at each of the node A, B, C and D to mimic or recreate a particle induced SET [20]–[24].

The Quatro 10T and the proposed 10T are capable of recovering from 1→0 as shown by the results in the Fig. 5.12 and Fig. 5.14 respectively for nodes A and B and Fig. 5.13 and Fig. 5.15 for nodes C and D. Fig. 5.12 illustrates that the capability of recovering from 1→0 SET which is introduced at node A.

As, we can see from the Fig. 5.12 node A after getting affected by the exponential current pulse is able to recover to 1. The sudden rise from 1 is due to the exponential pulse which we introduced at node A. The other nodes also seem unaffected from the Fig. 5.13.

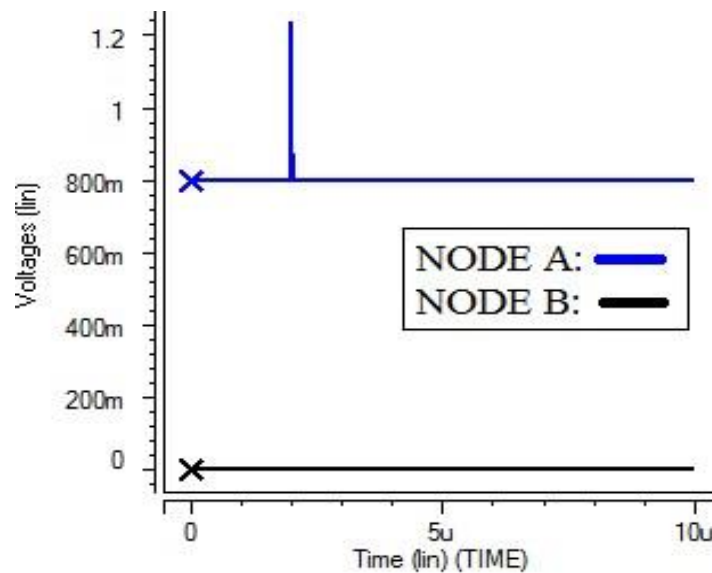


Fig.5.12. Simulation showing recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage selected based on current margin) a 1 to 0 at nodes A and B (for all values of current)

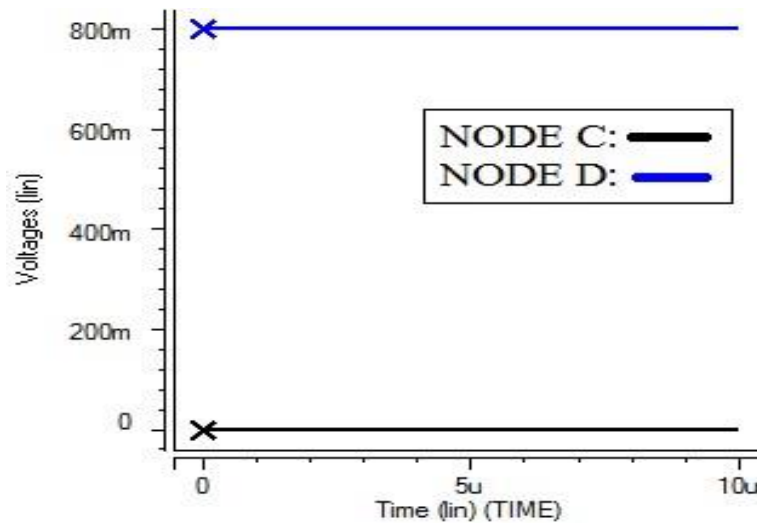


Fig.5.13. Simulation showing recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage selected based on current margin) 1 to 0 at nodes C and D (for all values of current)

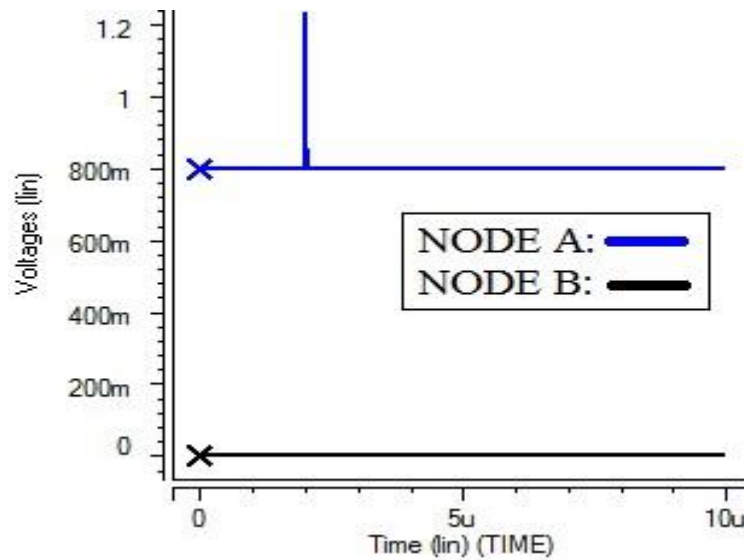


Fig.5.14. Simulation showing recovery of the proposed-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage selected based on current margin) 1 to 0 at nodes A and B (for all values of current)

The proposed 10T also shows a similar behavior such as the Quatro 10T cell which can successfully recover if 1→0 SET is introduced at node A. Both figures Fig. 5.14 and Fig. 5.15 seem similar due to the similar exponential pulse introduced at both places and the same supply voltage taken in both cases, but the nodes at which recovery occurred is different. Quatro and proposed 10T cell has the capability to recover from 1→0 SET at node A whereas a sufficiently large or strong 0→1 SET at node A can flip the cell. When a large 0→1 SET is occurring at node A $V_A = 0$, then N2 has the capability to turn the transistors P1 and P4 ON by reducing the value of V_C whereas N3 has the capability to

turn OFF N4 by lowering the value of V_B , in this way the cell is flipped. But the proposed 10T is made more robust against the 0→1 SET compared to that of Quatro 10T by replacing the NMOS access transistors by the PMOS access transistors in the proposed cell. The cell becomes more radiation hardened by using PMOS access transistors because the leakage currents in the PMOS access transistors do not get affected by the radiation bombardment whereas the leakage currents in NMOS access transistors increase rapidly which corrupts the stored data.

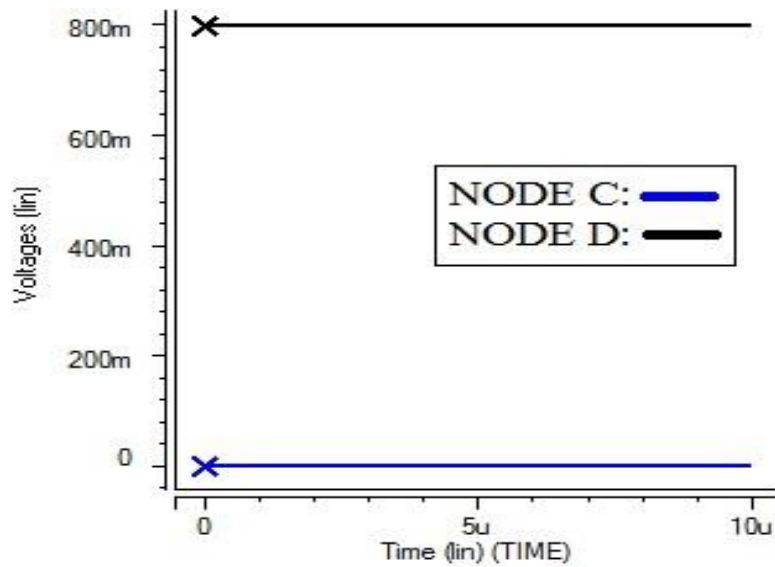


Fig.5.15. Simulation showing recovery of the proposed-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage selected based on current margin) 1 to 0 at nodes C and D (for all values of current)

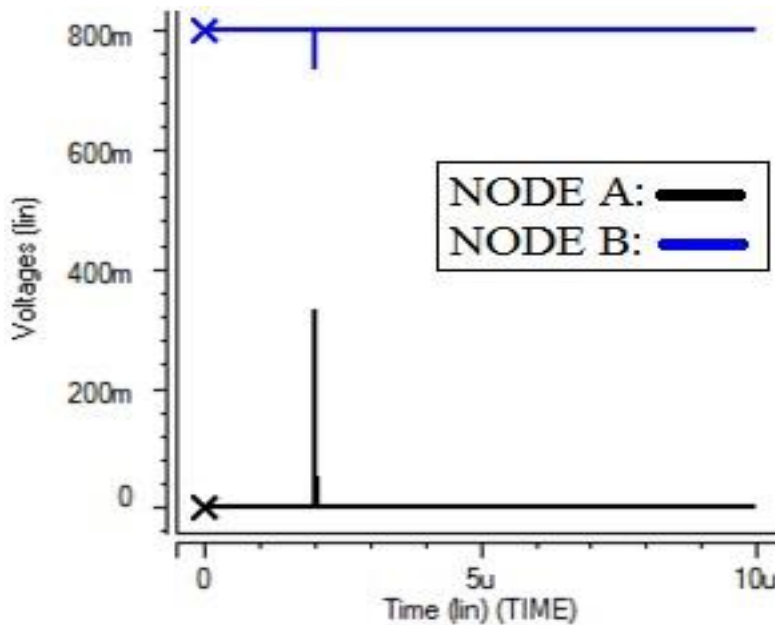


Fig.5.16. Simulation showing recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 229 μ A) 0 to 1 at nodes A and B

The parameter by which we analyzed the soft error robustness in this paper is current margin. Here, the term current margin is the maximum value up to which the cell can withstand the stored values without getting flipped when a SET is introduced at the nodes. For the Quatro 10T cell, the cell is able to recover from 0→1 SET until the value of current in the exponential current spike reaches 229 μA as shown in the Fig.5.16 and Fig.5.17.

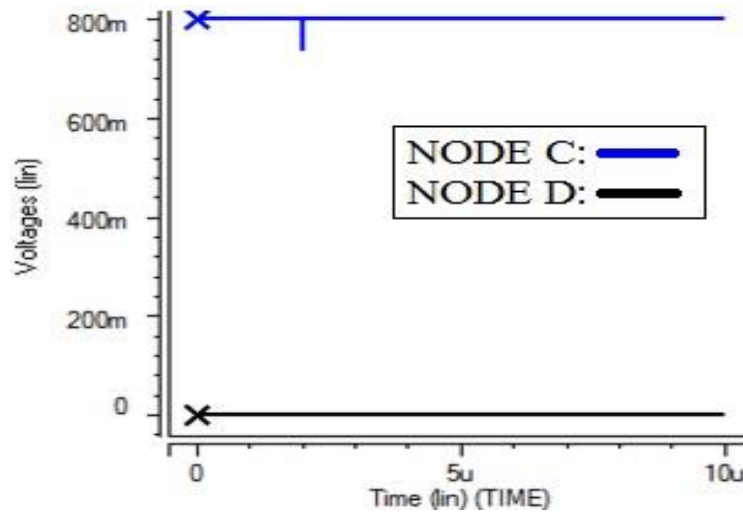


Fig.5.17. Simulation showing recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 229 μA) 0 to 1 at nodes C and D

Here, we can see from the Fig. 5.16 that nodes A and B, and from Fig. 5.17 nodes C and D are able to recover to their original values at 229 μA . Whereas if the current in the exponential current spike reaches 230 μA we can see that the Quatro 10T cell is flipped as shown in the Fig. 5.18 for node A and B and Fig. 5.19 for nodes C and D.

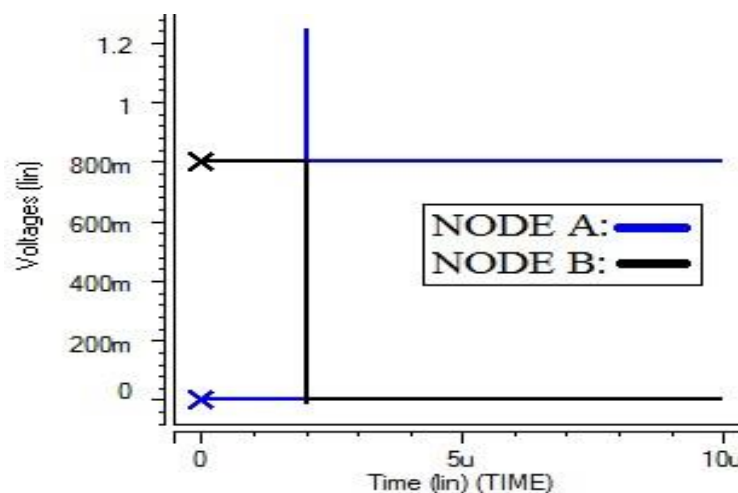


Fig.5.18. Simulation showing non-recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 230 μA) 0 to 1 at nodes A and B

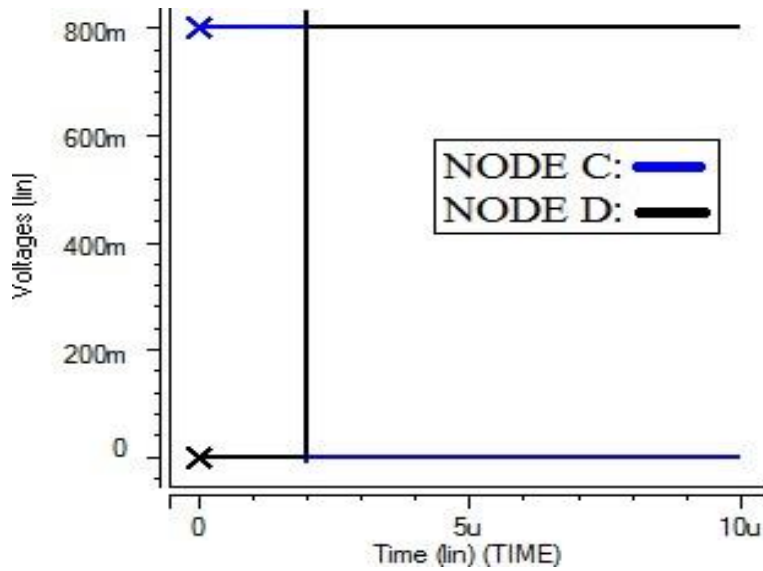


Fig.5.19. Simulation showing non-recovery of the Quatro-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 230 μ A) 0 to 1 at nodes C and D

From the above Fig. 5.18 and Fig. 5.19 we can see that the cell got flipped when 0 \rightarrow 1 exponential current spike reached the value of 230 μ A. It can withstand the stored values till 229 μ A. Therefore, the current margin for 0 \rightarrow 1 SET of the Quatro 10T cell is 229 μ A.

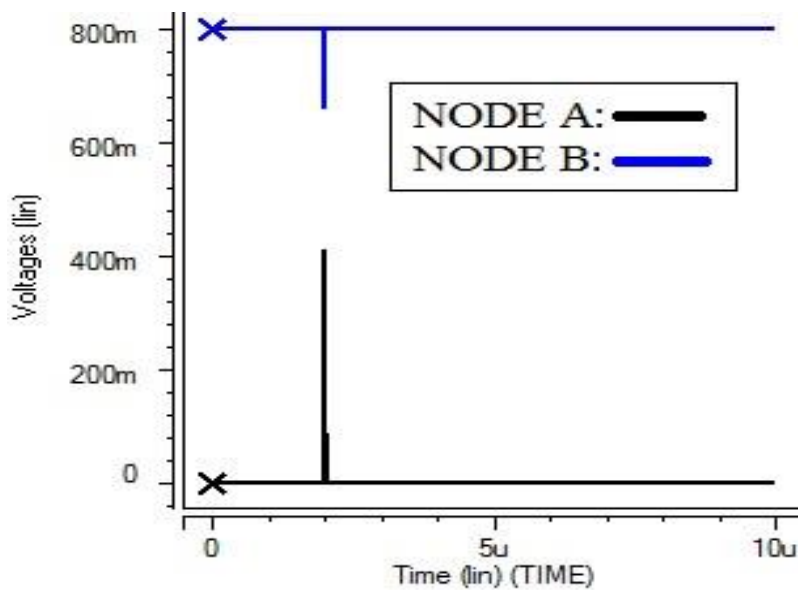


Fig.5.20. Simulation showing recovery of the proposed-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 232 μ A) 0 to 1 at nodes A and B

For the proposed 10T cell, the cell is able to recover from 0 \rightarrow 1 SET until the value of current in the exponential current spike reaches 232 μ A as shown in the Fig. 5.20 for nodes A and B and Fig. 5.21 for nodes C and D.

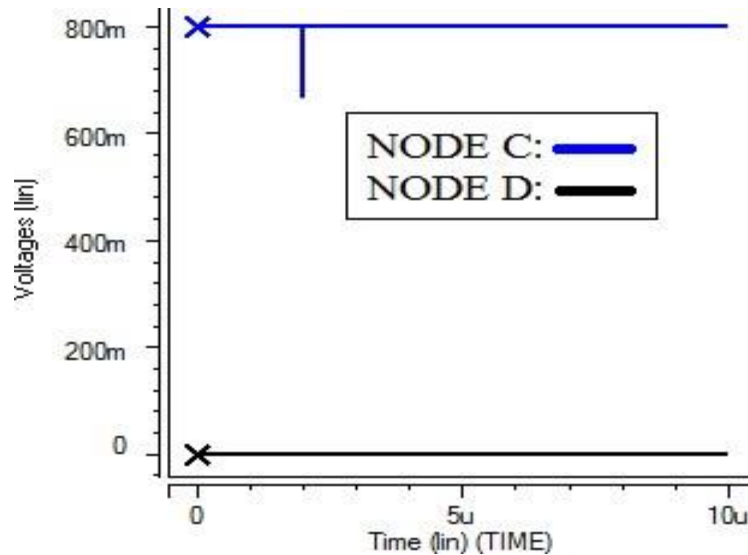


Fig.5.21. Simulation showing recovery of the proposed-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 232 μ A) 0 to 1 at nodes C and D

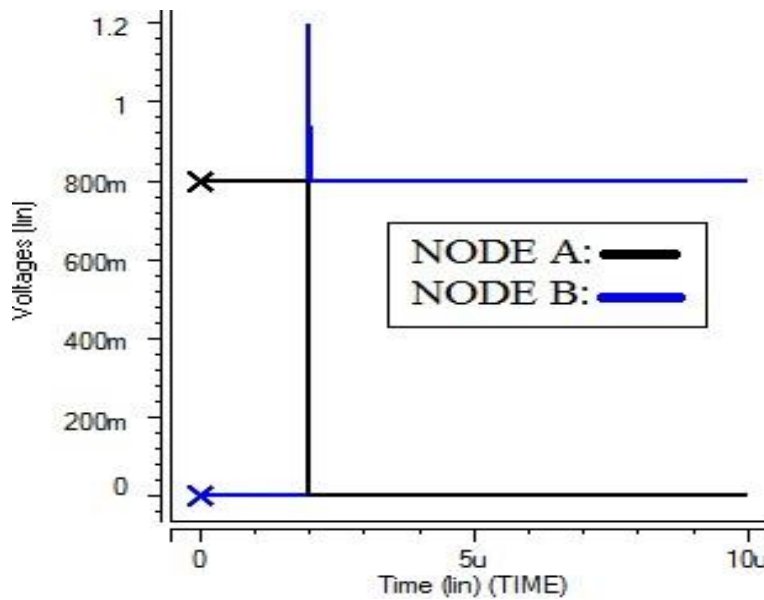


Fig.5.22. Simulation showing non-recovery of the proposed-10T cell for an exponential injected current mimicking (pulse width of 50 ns and peak voltage of 233 μ A) 0 to 1 at nodes A and B.

From the Fig. 5.22 and Fig. 5.23 we can see that the cell gets flipped when the value of current of the exponential current spike reaches 233 μ A. The proposed cell is able to withstand the stored values at all the nodes until 232 μ A. The current margin in the case of proposed cell is 232 μ A. Fig. 5.24 shows the enlarged version of the injected exponential current spike at node A for proposed cell just to show how the exponential current spike effects the nodes.

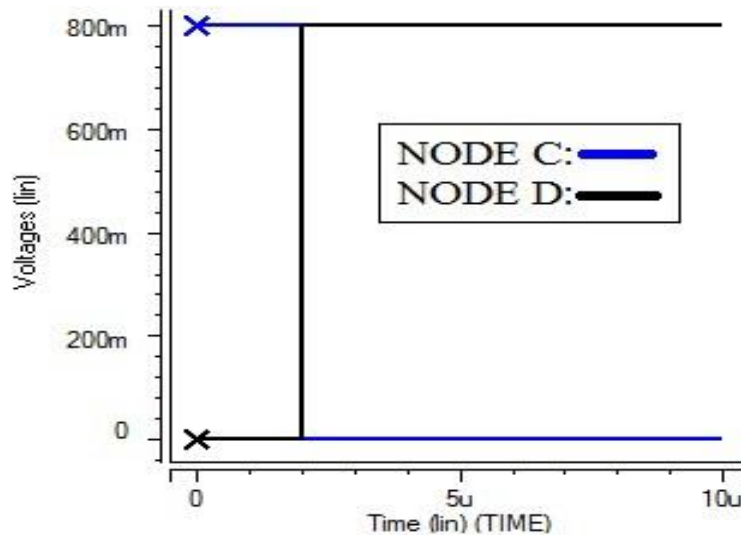


Fig.5.23. Simulation showing non-recovery of the proposed-10T cell for an injected exponential current mimicking (pulse width of 50 ns and peak voltage of 233 μ A) 0 to 1 at nodes C and D

Here, we can see from the Fig. 5.20 and Fig. 5.21 that all the nodes A, B, C and D are able to recover to their original values at 232 μ A. Whereas if the current in the exponential current spike reaches 233 μ A we can see that the proposed 10T cell is flipped as shown in the Fig. 5.22 for node A and B and Fig. 5.23 for node C and D. Therefore, we can observe that we have an increase in the value of current margin by 3 μ A in the case of proposed cell compared to that of Quatro cell. Therefore, the proposed 10T cell can withstand 3 μ A stronger 0 \rightarrow 1 SET compared to that of Quatro cell. This makes the proposed cell more robust for the soft error than the Quatro cell. The reasons for this robustness are mentioned in the above discussion.

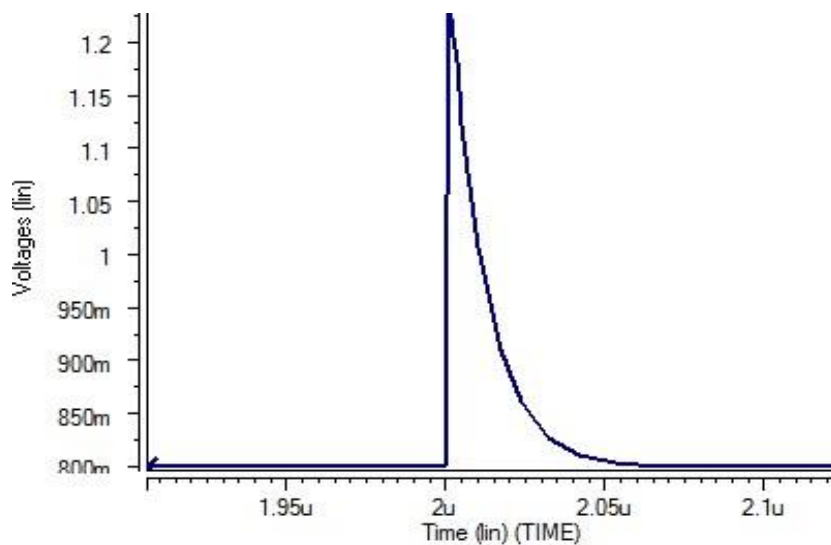


Fig.5.24. Enlarged version of the injected exponential current spike at node A for proposed cell (pulse width = 50 ns).

CHAPTER 6

CONCLUSION AND FUTURE SCOPE OF WORK

6.1. CONCLUSION

We have presented a 10T SRAM cell that uses PMOS access transistors, which is more soft error robust, compared to that of Quatro-10T cell at 22-nm technology. All the readings are taken with 5000 sample size while performing Monte Carlo simulation. The increment of $3\mu\text{A}$ in current margin implies that proposed cell withstands flipping to current spikes which are stronger which makes it reliable compared to Quatro-10T cell. The unaffected PMOS transistors leakage currents after radiation bombardment and hence usage of PMOS access transistors in proposed 10-T SRAM cell makes it more radiation hardened than Quatro-10T cell. The increment in current margin suggests the better application of the proposed cell in radiation environment or in aerospace industry. Therefore, the proposed cell remains as an attractive choice aerospace application.

6.2. FUTURE SCOPE OF THIS WORK

We need to find cell area of the proposed 10T SRAM cell and compare it with Quatro-10T SRAM cell. We can also reduce the cell area and make it more compact by reducing the cell ratios. We can also improve the Read Static Noise Margin (RSNM) by reducing or increasing the number of transistors. We can make it more radiation hardened by employing new designs. We can make the cell much more reliable by improving the current margin. It can be made to work with many other devices for wider applications.

APPENDIX A

ACCEPTED PAPER

International Conferences

REFERENCES